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# 2014 NA62 Status Report to the CERN SPSC

**Abstract**

NA62 aims to study the rare decay $K^+ \to \pi^+\nu\bar{\nu}$ at the CERN SPS. In this document we report the status of the detector construction and the general progress of the experiment since April 2013. The schedule for the completion of the construction and the preparations in view of the physics data taking in October 2014 are detailed. During the past year many major elements have been delivered, including the RICH vessel and the TDCpix ASIC. The production of the LKR CREAM modules has started and the manufacturing of the Straw chambers and of the LAV stations have continued steadily. All the Straw frontend electronics has been procured.

# Contents

# 1 Introduction

The main aim of NA62 is to address the measurement of the rare decay $K^+ \to \pi^+\nu\bar{\nu}$, a decay sensitive to new physics [1] via loop processes and well predicted in the Standard Model (SM) [2]. To appreciate an example where the study of $K^+ \to \pi^+\nu\bar{\nu}$ may probe energy scales beyond those accessible at the LHC, we refer the reader to [3] where the sensitivity to $Z'$ gauge bosons is considered under several scenarios. NA62 is built to improve the current experimental precision, $B(K^+ \to \pi^+\nu\bar{\nu}) = (1.73^{+1.15}_{-1.05}) \times 10^{-10}$ [4], by measuring kaon decays-in-flight with calorimetry to veto extra particles, very light mass trackers to reconstruct the $K^+$ and the $\pi^+$ momenta and full particle identification capability [5].

# 2 Technical Co-ordination and Schedule

## 2.1 Measurements of the magnetic field

Last summer the collaboration has made precise $B$-field measurements of the spectrometer magnet and of the residual B-field along the vacuum tank. A custom measurement bench (shown in Fig. 1) was introduced in the MNP33 dipole magnet and about $10^5$ data points were taken in a region of about $\pm 4$ m in $Z$ and in a diameter of about 2 m in $X$,$Y$ covering the central field region and the fringe field at the periphery of the magnet. Results of these measurements are shown in Fig. 2.

Given the long extrapolation required to reconstruct the kaon decay vertex in the decay region, it is important to note that we are sensitive to residual magnetic field present in the decay tank. For this reason a campaign of measurements was made over a length of about 80 m to measure the $B_X$ and $B_Y$ components of the integrated field. Thanks to these measurements (shown in Fig. 3) the uncertainty of the integrated $B_X$ and $B_Y$ components is now known to a level of $2 \times 10^{-4}$ Tm, which is sufficient for the physics.

## 2.2 Present Status and Plans until October 2014

The construction and installation of the NA62 experiment is entering the final straight before its first physics data taking this autumn. At this moment all groups are fully

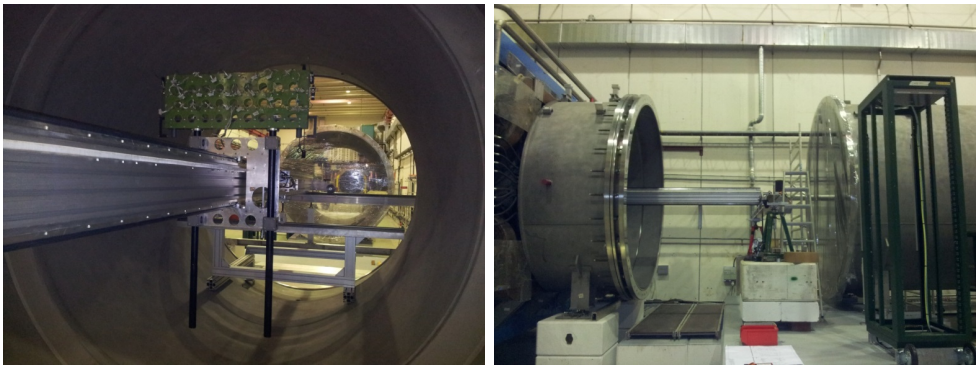

Figure 1: B-field measurement bench as it was introduced in MNP33

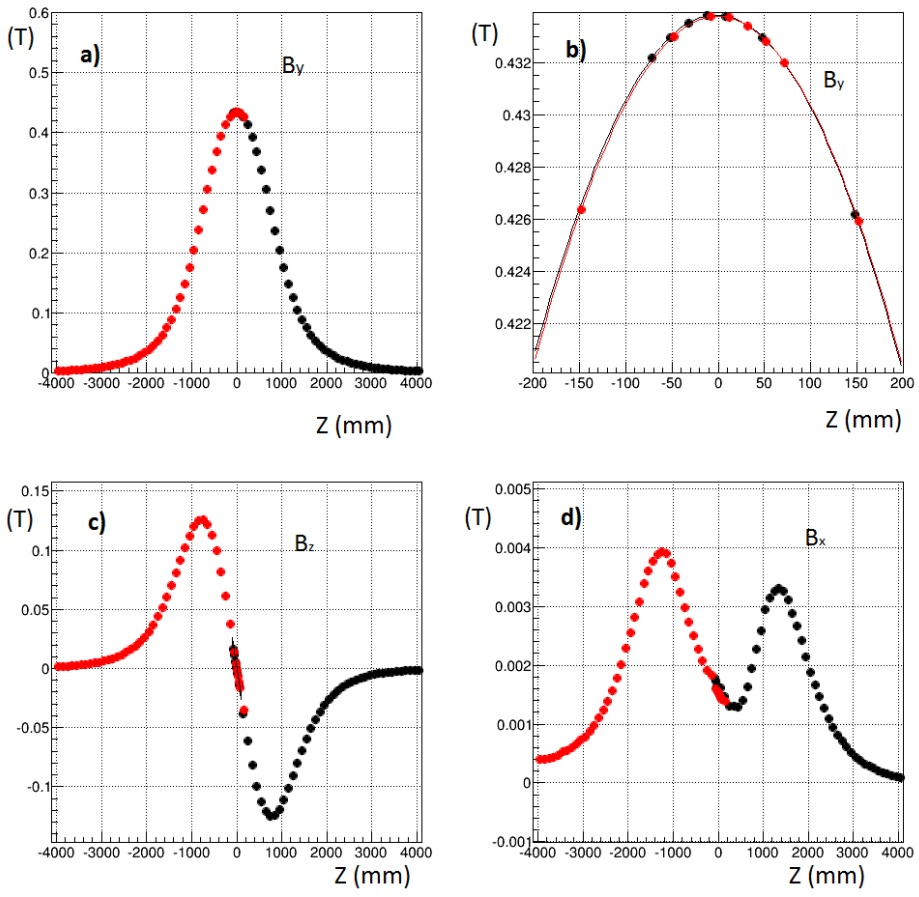


Figure 2: Examples from the B-field measurements: a) $B_y$ (X=28 cm, Y=44 cm) versus Z; b) same as a) with zoomed scales; c)$B_z$ (X=28 cm, Y=44 cm) versus Z; d) $B_x$ (X=28 cm, Y=44 cm) versus Z. Note: Z=0 is in the centre of the magnet

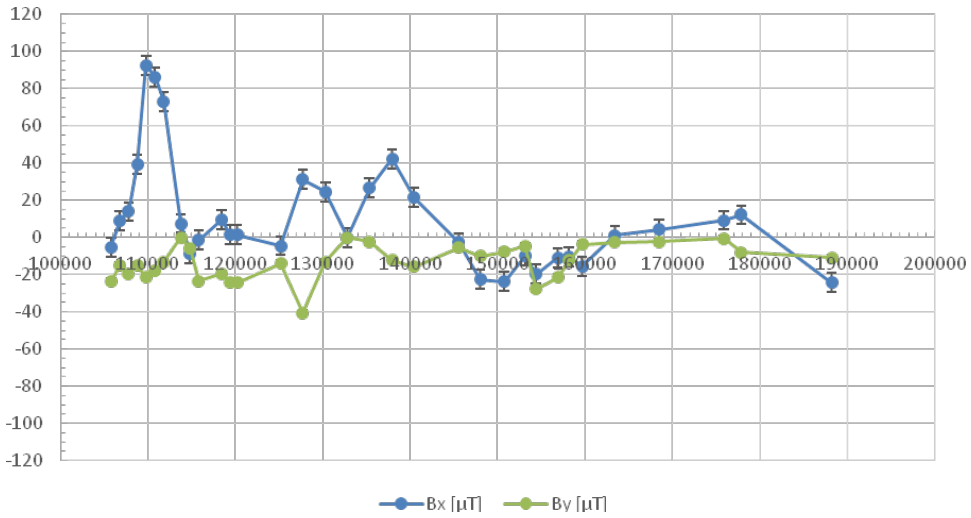


Figure 3: Residual B-fields in $B_x$ and $B_y$ in the vacuum tank over a length of 85 m. The horizontal axis is the Z axis of the experiment in mm, starting shortly after GTK3 and ending after the MNP33 magnet. The MNP33 magnet was off during these measurements

engaged in completing the construction and installation of the detectors in time for the commissioning. The installation schedule of the detectors is shown in Fig. 4. The progress over the last 12 months has been on schedule, and we are confident that the few delays which have occurred for some deliverables (e.g. RICH vessel and vacuum tubes 26 and 28) can be recovered before the run. Confirming the importance of the allocated beam in 2014, we give here a short status report for each sub-system.

- The **KTAG** is installed; completion of the photo-detectors and readout is ongoing.
- **GTK:** the ASIC has been fabricated and first tests show that the chip is working as expected. The chip thinning and bump bonding has been successfully tested on dummy chips. The detector assembly with the micro-channel cooling plates has been tested using dummy components. Remaining work is on a tight time plan, but the most difficult technical issues have been mastered and we believe that it is feasible to install a first version of the full size detectors for the run in October.
- **Straw Tracker:** the module assembly is completed at CERN (4/4 modules completed) and coming to an end at JINR (3/4 modules completed, the last module will be finished in June). The frontend electronics were all produced and successfully tested. The "dressing of the chambers", i.e. attaching all services (HV,LV and gas patch panels) to the chambers is in full swing. The SRB (back-end electronics) development is coming to the end and the production of a pre-series is expected to start in May 2014.
- **RICH:** the 17 m long vessel (see Fig. 5) has been installed and leak tested. The aluminisation of the mirrors is ongoing at CERN ($\approx$ 60% completed) and will be finished in time for the installation. The design and testing of the mirror mounts has been successfully accomplished. On the critical path is the delivery of the mirror support panel (expected end of April). Mirror installation and alignment will start immediately afterwards.

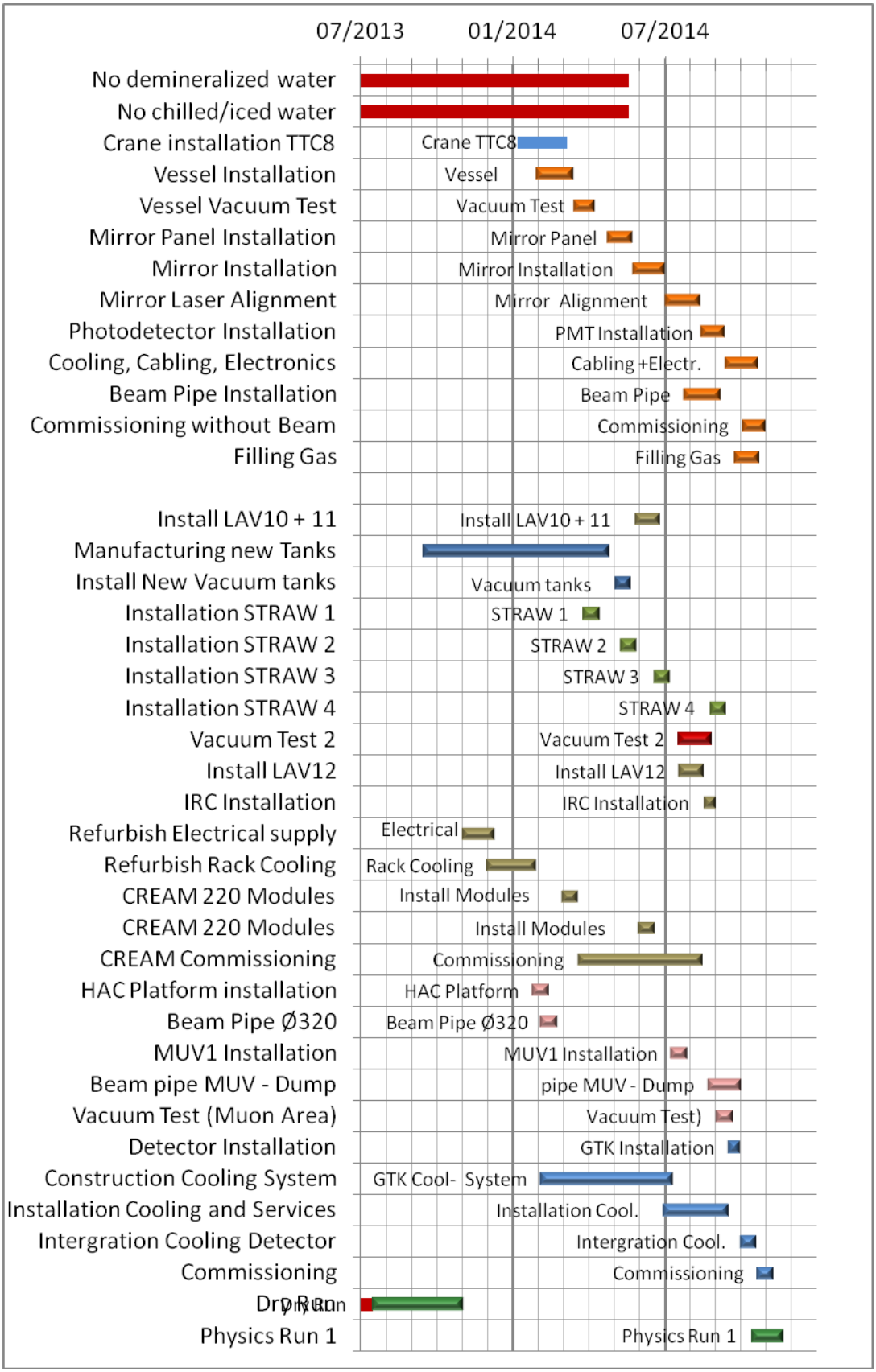


Figure 4: NA62 Installation Schedule

- The **Aluminium Beam Pipe** (20m long) is in fabrication in the CERN central workshop. The machining of the pieces is completed, the welding work is on schedule ($\approx$ 55% completed). The installation is foreseen this summer.

Figure 5: Unloading of the $3^{rd}$ RICH vessel in EHN1

- **LKR / CREAM readout:** The tests of the CREAM prototypes last year have been very successful and the production (at CAEN) of the all modules will be in line with the schedule. The cooling system and the electrical infrastructure for the CREAM racks were redone. We expect to install all modules by July this year.
- **Infrastructure:**
  - The delivery of the two remaining vacuum tanks (tanks 26 and 28) was delayed by 3 months; their installation has been shifted to beginning of May.
  - The Straw Chamber interface pieces (for chambers 2+3) have been received. The order for the interface of Chamber 4 has been placed.
  - A new crane was installed in TCC8 this winter. Both overhead cranes (TCC8 and ECN3) correspond now to state-of-the-art technology and meet our needs for the detector installation.
  - The electrical installations and the optical-fibre network for the detectors have been completed this winter.
  - The contract for the PC farm cooling system was signed and the installation work is ongoing.
  - Intensive cabling work for the new vacuum system is ongoing and all valves and pumps have been delivered to CERN. A thorough test of the vacuum system is scheduled for July.
- All **LAV** modules (1-11) that are part of the vacuum tank are in ECN3: LAV1-9 are installed, LAV10+11 will be installed after the installation of the neighbouring vacuum tubes(26+28). LAV12 (located outside the vacuum tank) will be installed in August.

- **MUV2+3** are installed. **MUV1** is under construction in Mainz. Some, unforeseen, difficulties on the mechanics and on the fibres delayed the construction of MUV1. The problems have now been solved and the construction resumed. The installation of MUV1 has been shifted to the summer and this can be accommodated within the schedule.

- **IRC and SAC:** the SAC is installed; the IRC is being assembled in Frascati. The installation is foreseen in August.

- The **Beam Line** had already been completed and commissioned for the technical run and only minor refinements are being implemented.

# 3 CEDAR / KTAG

The main work in 2013 and 2014 builds upon the achievements of the technical run in 2012 with four functioning light boxes, and aims to complete KTAG with eight fully functioning light boxes and prepare for the data taking in October 2014. We plan to have the KTAG completed in all its aspects and tested with LED and pulsers by the end of August 2014.

## 3.1 Mechanics

Following the experience of the technical run in 2012, a few modifications were made to KTAG. The ring on the mirror cylinder that locates and orientates the optical fibres to illuminate each mirror has been modified to make installation of the fibres simpler and more secure. The ATEX cylinder has been modified to simplify the reintegration of KTAG and the opening/closing of the two halves. The optical stages have been modified to allow for the exchange of the mirrors needed for the 48 or 64 PMTs configuration; the stage now enables precise movement of the mirror to give the necessary shift in the reflected Cherenkov light pattern in both X and Z directions to accommodate for both configurations. Besides, the eight lenses covering the quartz windows were replaced; the LED system and new mirrors and ATEX cylinder were reinstalled; stainless-steel panels insulated by fire-retardant, were fitted around the support cylinder, thus completing the insulation system; and the temperature sensors were calibrated. The two halves of KTAG were reintegrated in summer 2013 and the cooling system tested again. From the mechanical point of view, the KTAG is fully ready for data taking.

## 3.2 Photomultipliers and readout

The Hamamatzu PMT R9880, as successor of the R7400, was tested and we found that its performances are equivalent or better than those of R7400 (higher gain, higher QE, same active area and maximum anode current). Several tests were performed in realistic conditions and the achievable time resolution and noise level were found to be comparable. A non-optimised NINO frontend threshold used in the technical run has been identified as responsible for the majority of the difference between observed and predicted number of photons per kaon; during the technical run it was not possible to adjust the threshold due to a now overcome limitation in the Detector Control System (DCS). The increased gain of R9880 will make the system insensitive to the threshold settings, for a large interval

of possible threshold values. Beside the increased QE will allow for a larger number of photons per kaon to be collected. Therefore a hybrid configuration, with 16 R7400 and 32 R9880, has been adopted (as shown in Fig. 6). PCBs sockets, modified for the R9880 PMTs, are been fabricated.

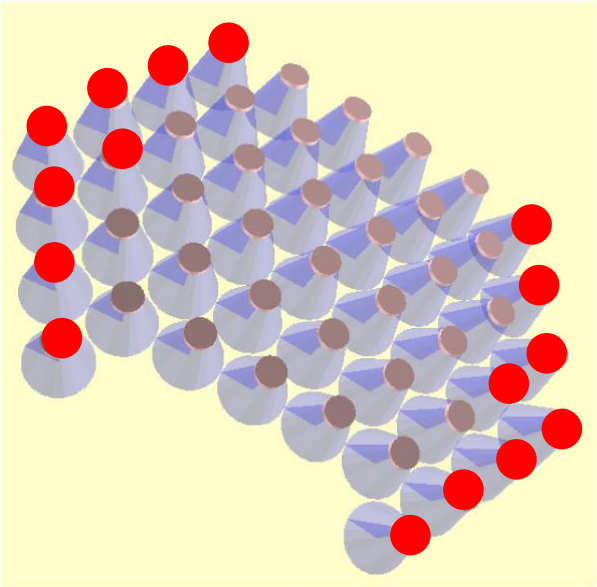

Figure 6: The PMT hybrid matrix. The position of the 16 R7400 PMTs are highlighted in red

Although the light illumination due to LED test system is rather uniform on the PMT plane, its exact uniformity is difficult to measure; therefore the equalization of the PMTs will be performed during a series of laboratory tests, using the blue index and gain data given for each PMT and a calibrated PMT from Hamamatsu; there is in fact a linear relation between the QE and the blue index. During these laboratory tests, the time performance will also be measured for each PMT using a laser. These tests are on-going.

The NINO boards have been modified to allow for the remote setting of the NINO threshold and voltage via DCS, and for more robust connectors. Two boards have been tested already and found to be fully functioning; the rest will be produced by RAL and tested at CERN by the end of April 2014. The NINO mezzanine chips, designed and produced at CERN, have the same functionalities but were reduced in size. While this has the advantage of being compatible with a better connector, the initial yield of good chips was rather low. However, after modifying the production technique, the yield has become close to 90% and we have already a number of fully functioning mezzanines sufficient to equip the whole KTAG plus a few spares.

During a dry run in 2013, the rate limitations were investigated using a front-end pulser; the two main limitations were found to be: HPTDC 40 MHz overall bandwidth and HPTDC channel occupancy of a few MHz per group of eight channels sharing the first latency buffer. Such limitations will be overcome with the design of a splitter that will allow to optimise the rate distribution over channels. With the use of the splitter, only four PMTs per HPTDC will be connected with a maximum rate of 5 MHz, and the

word rate per whole HPTDC (leading and trailing) will be limited to about 30 MHz. A passive 9U splitter board has been designed and boards fabrication is on-going at RAL.

To satisfy the rate requirements, the possible radii of curvature of the mirrors have been investigated using a simulation and it has been found that both 51.68 mm and 39.24 mm give satisfactory results. Therefore both sets of mirrors will be prepared and available for the data taking in October 2014; the mirror with the bigger radius will be used as default, since it gives a higher number of photon per kaon. In case the rate will be proven to be too high, the mirrors with smaller radius will be installed (the installation will take only one day).

The residual inefficiency observed in the KTAG readout during the technical run was not due to high rate (the beam intensity at the time was significantly lower than the nominal intensity) but appears to be linked to a contingent, not optimal timing of the TDAQ; this issue is currently under investigation.

Finally, the TELL1 and TEL62 will be tested during a radiation exposure at RAL in the early part of 2014; a preliminary test was conducted and no effect has been seen due to the integrated muon flux corresponding to the equivalent NA62 fluence. The following step, to be performed at the end of March, will concentrate on the detection of possible single-event-upset and data corruption with a muon exposure.

## 3.3 Detector Control System (DCS)

The KTAG branch of DCS is responsible for aggregating all the information from the various hardware components of the KTAG and based on the state of these reporting an overall state of the sub-detector. The hierarchy of which is depicted in Fig. 7.

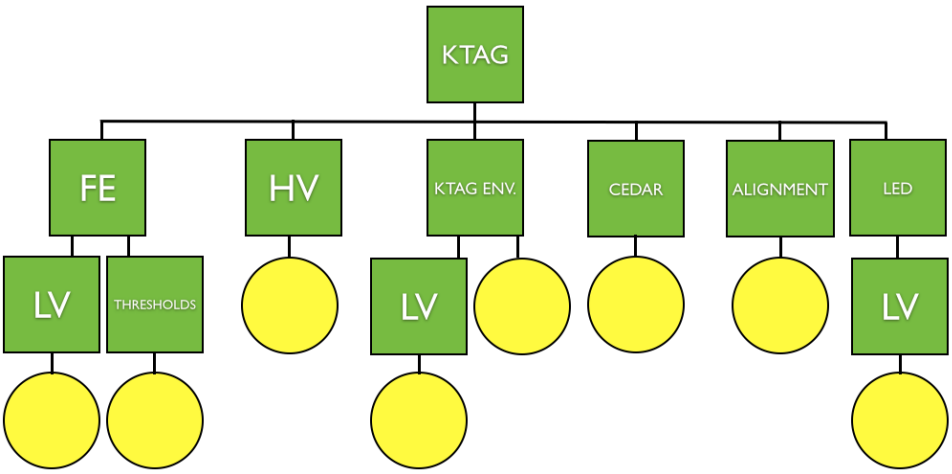


Figure 7: The KTAG DCS hierarchy

Each of the green boxes is a component in the DCS and has a fully functioning graphical user interface. The yellow circles indicate connections to the hardware i.e the high voltage (HV) is connected to CAEN A1536 high voltage PSUs. The front-end electronics (FE) node has been tested on hardware and is complete. This includes a low voltage module, which has a driver developed by NA62 UK based on the DIM protocol, this allows a connection from the front-end server to the KTAG DCS project.

The KTAG component of the DCS is unique in that it has to interface to some non-standard hardware, where non-standard indicates it is outside the JCOP framework developed at CERN for detector controls. The most complex is the Gas Control System

(GCS) responsible for pressure control of the CEDAR vessel. To allow communication across the two systems the NA62 UK team generated an interface contract based on the DIP protocol to allow control commands to be issued from the DCS, without directly controlling the hardware, which is under the remit of the GCS. The series of commands and command handling has been tested on a local system and is due to be interfaced to the GCS at the beginning of April.

To summarise, the core components of the DCS have been tested on hardware and work correctly, including a fully functioning finite state machine for each. The non-standard components are moving to the hardware testing phase within the next month. The NA62 UK team has delivered the FE node and the LV node based on a bespoke DIM driver and is responsible for building the interface to the GCS to allow control of the pressure of the CEDAR vessel.

# 4 GigaTracKer (GTK)

In 2013 and beginning of 2014, major steps have been achieved and most of the technical challenges have been addressed. Several aspects, which are discussed in more detail in the following text, are here briefly summarized.

- The ASIC chip (TDCpix) has been received and electrical tests have started: so far all the functionalities have been shown to work as expected.
- The chip thinning and following bump-bonding has been achieved at IZM, Berlin. Several single-chip assemblies have been fabricated: mechanical and electrical tests are underway.
- The feasibility of the micro-channel cooling has been demonstrated.
- The DAQ ("Off-detector" electronics) prototype cards have been fully tested and are under production.

With some optimism, one can say that the schedule can be kept: but, to have at least three full stations by October, no slippage is allowed. Details on the above achievements are discussed in the rest of this section.

## 4.1 TDCpix ASIC

The TDCpix ASIC was submitted in June 2013 to the IBM foundry for fabrication. Intensive full ASIC and GTK hardware simulations have been performed as part of the sign-off routine. A fully automated test bench for the TDCpix ASIC has been built up. This test bench is based on a commercial FPGA processor card connected to a custom carrier board which allows to plug in a daughter board carrying the TDCpix directly wire bonded to the PCB. The hardware has been delivered end of December 2013. The software has been designed in advance and to a large extent been extracted from the ASIC design simulation test bench. This allows a double use of the software routines for the ASIC production sign-off routines and the verification of the final ASIC. The tests are proceeding quickly and presently all tested functions are working, meeting or exceeding specifications.

## 4.2 GTK carrier

The GTK carrier has been designed according to the pad layout of the final TDCpix submission and the GTK general integration scenario. Intensive signal integrity simulations for both the high speed signal and the power plane have been conducted. Due to the complexity and the high number of long high speed signal lines on the PCB close collaboration with prospective manufacturers has been established. The layout of the boards have been optimized in order to enhance production feasibility and yield. Mechanical integration studies with the cooling/mechanics team have been performed. An internal design review has been organized in order to verify specifications and performance. Presently a first batch of pre-series boards is about to be produced.

## 4.3 Bump bonding

During March/April 2013 the tender document for the supply of bump-bonded Si pixel assemblies has been prepared. The tender document specified all the requirements of the supply in terms of quantities, technical specifications, acceptance tests and schedule. The supply foresees a pre-series composed of thinned and bump bonded assemblies made of dummy components, and a production-series for the delivery of full-detectors and single-chip assemblies thinned and bump-bonded. The purpose of the pre-series is to develop the required expertise for the chip thinning and bump bonding. The Tender has been addressed to two Institutes of Research, Fraunhofer IZM (Berlin) and VTT Technical Research Centre of Finland, previously qualified in a tailored Market Survey (MS-3651/PH/NA62). Valid offers from IZM and VTT were received by May, 22nd and opened on May, 28th. All the technical exceptions included in the offers were analyzed and accepted on June, 4th, and the IZM offer unanimously accepted during the adjudication meeting held the same day.

At the beginning of July we held a kick-off meeting with Ing. Thomas Fritzsch, the IZM contact person, where all the technical details of the project and the test procedures were discussed. The schedule envisaged a period of six months devoted to the pre-series, once the dummy sensors and read-out chips with custom daisy chain were available at IZM. At the beginning of August the daisy chain technical files for the dummy modules were sent to IZM, and by mid September the dummy sensor and read-out wafers were ready for the subsequent processing steps.

At the end of the year, the first thinned and bump-bonded single chips were produced, just before a one-month forced stop of the bump-bonder tool at IZM. The current status of the pre-series is that all the sensors and read-out wafers are prepared/diced and thinned (read-out wafer) and all the bump-bonding processing steps have been tested. The bump-bonding of all single chips and full detectors are ongoing. Also the glass carrier removal step has been tried on some chips. Metrology measurements and functional tests, before and after thermal cycles, are under preparation and will follow in the next month. Part of the tests will be repeated at CERN.

The pre-series work schedule has been heavily affected by a general maintenance and renovation campaign ongoing at IZM during fall. We have accumulated a two months delay with respect to the original schedule. We should be able to evaluate the quality of the bump-bonding on the dummy modules by the end of May. The production-series will be launched right after. The time foreseen for a first batch of full detector assemblies is of the order of three months.

## 4.4 Micro channel cooling

**Progress during the past 12 months**

One of the six cooling devices produced by IceMOS was diced, locally thinned and metalized in the EPFL CMI clean room by PH-DT, and finally equipped with a first generation of soldered connectors at CERN (Fig. 8). The device has then been equipped with a silicon thermal mock-up simulating the sensor and the 10 chips and tested in the PH-DT vacuum vessel.

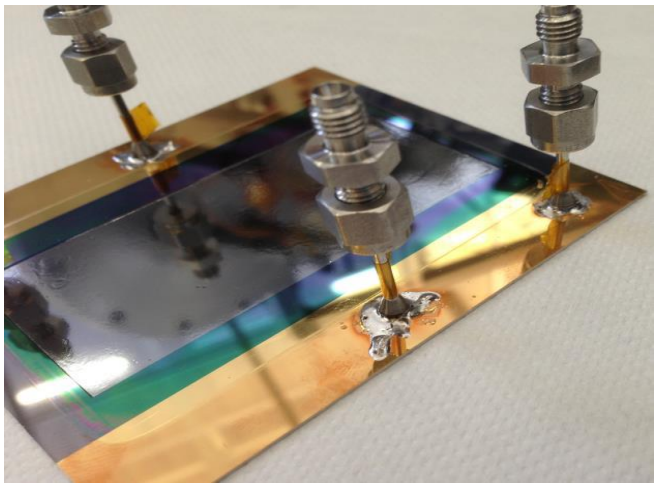

Figure 8: One device from the IceMOS production, post-processed by PH-DT, prior to installation in the test vessel for thermo-hydraulic characterisation

The global procedure for the final integration of the assembly "cold plate + GTK module" ("cold module") onto the PCB and into the GTK vessel has been finalized. Seven "work packages" have been identified:

- WP1 - Microfabrication of Cooling Plates
- WP2 - Fluidic Connectors
- WP3 - Tubing
- WP4 - Cooling Plant (interface to the design and procurement task assigned to EN/CV)
- WP5 - Thermal Interface
- WP6 - Assembly to PCB + Wire-Bonding
- WP7 - Vacuum Flange + Vessel (interface to the vessel lids)

Good and steady progress has been made on all the WP's:

- **WP1:** Although the etching and bonding quality observed on the IceMOS prototypes is fully satisfactory, the company is not able to commit for the complete processing of the final devices, not being able to accept engagements on the critical steps of dicing, local thinning and metal deposition. Performing all these post-production steps in the EPFL CMI clean room, with the limited level of control and repeatability typical of an R&D university facility, is only possible at the prototype level, not for the final production. An alternative provider has been identified in CEA-LETI 3S, who has recently completed with success the pre-production of LHCb VELO micro-cooling devices. The design and fabrication process has been studied and validated by CEA-LETI 3S, who is ready to engage on the full production with a minimal guaranteed yield of 50%. A Rough Order of Magnitude quotation has been agreed, and a firm offer is expected soon. The order will be launched immediately and a first minimal lot of 10 devices is expected by summer. In the mean-time, the remaining five devices produced by IceMOS will be post-processed by PH-DT and will be available as back-up.

- **WP2:** The epoxy glued PEEK hydraulic connectors used in the prototyping phase have been replaced by miniaturized metallic connectors soldered to the silicon surface. The final solution adopts minimal size connectors made in Kovar, a metallic alloy with a CTE very close to the one of silicon. The vacuum brazing procedure has been developed in collaboration with EN-MME. Prototype connectors brazed to silicon have been successfully tested for leak tightness and mechanical resistance to pressures in excess of 700 bars (Fig. 9).

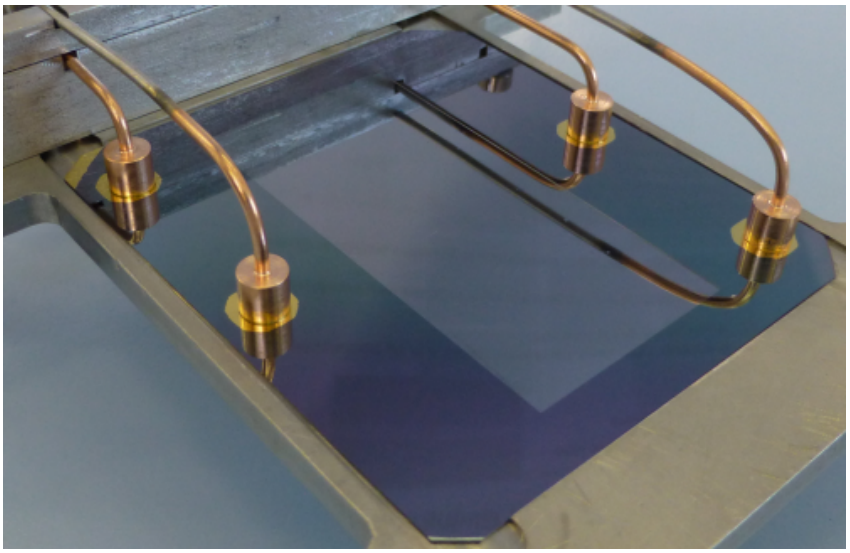

Figure 9: Miniaturized soldered Kovar connectors

- **WP3:** A flexible design for the metallic tubing inside the vacuum vessel, including manifolding and feed-through, has been identified: it allows compensating for all pipe contractions and/or expansions due to temperature changes in excess of 50°C. Specific tools for pipe bending have been fabricated and sets of tubes realized for trial assemblies and dimensional verifications (Fig. 10).

- **WP4:** The interfaces of the local thermal management device with the GTK cooling plant have been agreed upon with EN-CV. In particular:

- The boundary of responsibility (the latest Heat Exchanger mounts on the support of the GTK vessel),
- The pipe interface from the Heat Exchanger to the entrance of the vessel (swap from 6 mm stainless steel pipe to 1/8" with VCR connection and a final filter),
- The test pressure for the final commissioning of the fully assembled system prior to operation (18.4 bars).

The tender for the cooling plant was adjudicated.

- **WP5:** After mechanical and irradiation tests, and validation with the final assembly jig and real scale mock-ups, the 30 $\mu$m thick adhesive film 3M 9461P has been selected as interface between the silicon cold plate and the GTK module.
- **WP6:** The whole procedure of integration of the "cold module" onto the PCB and of wire-bond execution has been frozen. The jigs are presently in fabrication for a complete validation of the whole integration process with a mechanical mock-up.
- **WP7:** The sealed flange ensuring the interface with the lid of the GTK vessel has been designed based on the experience cumulated in PH-DT with the very similar flanges successfully developed for the Roman Pots of the TOTEM experiment. The work is steadily progressing in parallel to the integration activity of WP6.

**Foreseen activities to completion**

Submission of the order for the procurement of the final micro-cooling devices with CEA-LETI 3S. Follow-up of the production and LETI and validation / acceptance of the produced devices (expected by summer). Complete post-processing of five IceMOS devices, one for long term testing/cycling in the PH-DT facility (by April) and four as back-up ready for installation in case of production delays at LETI (by June). After the complete validation of the integration procedure on mechanical mock-ups, revision of all technical details and execution of the final integration on the first three modules for installation in the experiment during summer (Fig. 10).

## 4.5 "Off-detector" Electronics

The off-detector electronics has the main task of receiving the data pushed by the TDCpix ASICs, save it on temporary buffers for the L0 trigger latency time, select the GTK data matching the L0 trigger request and send packets of events to the sub-detector PCs. These functions are performed by electronic modules dubbed GTK-RO.

Each "on-detector" ASIC is served by one GTK-RO module. The latter is actually made of two decked units: the mother board, which is a 6U VME card hosting the main functional blocks, and a daughter card featuring the interface to the TTC system and various timing functions required for the operation of the connected ASIC. In the course of 2013 the firmware for the FPGA was upgraded to instantiate a newer version of the DDR2 external memory controller to take advantage of the upgraded diagnostic resources offered by the 12.1 release of the ALTERA FPGA development suite. The new "External memory interface toolkit" in particular has allowed to solve issues connected with the power-on calibration phase of the DDR2 SDRAM controller. The firmware upgrade of the GTK-RO FPGA also had the goal to prepare internal emulators of the basic data links to and from the "TDCpix" ASIC and to debug the interface to the trigger/timing

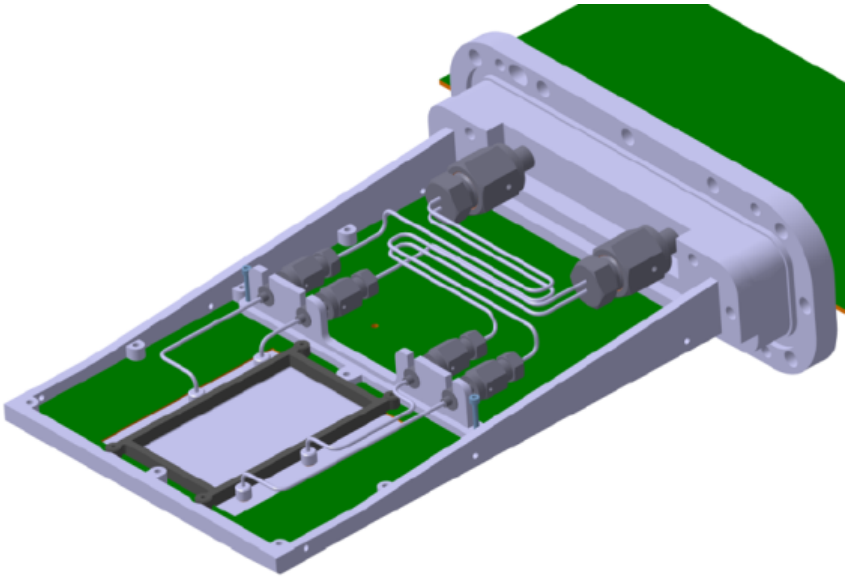

Figure 10: Integration of the "cold module" onto the GTK PCB, including the tubing and the sealing flange

signal delivered by the TTC system. The features illustrated above have been exploited in the course of a dry-run in November 2013 at NA62. In preparation for the dry run, a sub-detector TTC system was also assembled in a VME crate containing a VME CPU, a "Local Trigger Unit" module and a TTC-ex optical fanout. Two prototypes of GTK-RO module equipped with TTCrq receiver modules (through temporary adapters) have been used during the test run to simulate the generation of 3.2Gbps data streams from a dummy TDCpix instance as well as the loopback of "slow control data" through the optical fibers actually installed in NA62. It was also verified during the dry run that the GTK-RO firmware would respond to the L1 triggers generated by the sub-detectors TTC systems with the generation of multi-event UDP data packets toward the subdetector PC. During the dry run a communication test between subdetector PC and DCS based on the current data structure for GTK was carried out.

After the dry run the order for the production of the GTK-RO motherboards (35 units) was signed off. The definition of the schematic of the GTK-RO daughter cards and high precision timing unit has proceeded with performance tests for the qualification of its key components and it has been finalized. The daughter card prototype production has been launched.

Concerning the hardware development, the activities foreseen from now until the 2014 run are:

- verifying the operation of the links between the GTK-RO mother board and the real TDCpix ASIC;
- performing quality acceptance procedures on the GTK-RO production boards;
- install and test operation of the off-detector system in the field.

Concerning the software development, the activities foreseen from now until the 2014 run are:

- implementing and benchmarking the "event assembler" code running on the sub-detector PC to receive data from the GTK-RO cards and push it to the PC-farm;

- implementing the Ethernet-based slow control link between the subdetector PC and the GTK-RO cards connected to it;
- testing the implementation of the communication protocol, based on DIM, between the subdetector PC and the DCS.

### 4.6 Mechanics and other activities

- GTK1 and GTK2 vessels: the design is finished and one prototype tested during technical run in 2012. Two extra vessels in production (one spare). They will be delivered to CERN by June 2014. As a remark, GTK3 is machined at Napoli together with the CHANTI.
- Wafer characterization: wafers have to be characterized to tag the on-board chips as OK-KO. The project to develop the probe card is ongoing and schematics are ready. The PCBs should be ready by mid-April
- In fact the characterization of a couple of wafers should be largely sufficient, being necessary somewhat like 30 chips to complete three stations (full detector) as a single wafer carries 70 chips.

## 5 CHANTI

The CHarged ANTIcounter detector aims at reducing the background induced by inelastic interactions of the beam with the last GTK station, GTK3. It detects the charged particles produced on GTK3 and emitted at relatively high angles with respect to the beam (while the rest of NA62 will be able to detect particles emitted at angles $< 49$ mrad). It is composed of six $300 \times 300$ mm$^2$ shaped hodoscopes with a $95 \times 65$ mm$^2$ hole in the centre to leave room for the beam. Each CHANTI station is made of scintillator bars (of triangular section) read by means of WLS fibres coupled to Hamamatsu Silicon Photomultipliers (SiPM). During the year 2013, after completing the analysis of data taken with a prototype station during the 2012 technical run, the activity on the CHANTI has concentrated on the construction and test of the system, on the procurement of the frontend electronics and on the development of the Monte Carlo simulation of the detector.

### 5.1 Construction and tests

The final design of the vacuum vessel hosting both GTK3 and the six CHANTI stations has been completed. It is made of two rectangular shaped stainless-steel chambers joined by a 670 mm long tube (diameter of 324 mm) welded on both sides to the two chambers, so as to form an unique 2160 mm long vacuum tight vessel. Both chambers are equipped with flanges and SUB-D 37 feed-through to allow for SiPM signals to be carried out towards the Front End Electronics (FEE) boards. Both rectangular chambers and the intermediate pipe have been already manufactured, and the final assembly and welding of the parts is scheduled to be done in Napoli mechanical workshop during April 2014.

All of the $\simeq$ 300 bars (including spares) needed to build the detector have been machined and assembled in Napoli. Each bar has been individually tested during a 6 h long cosmic rays data taking in a climatic chamber, in order to be validated for the

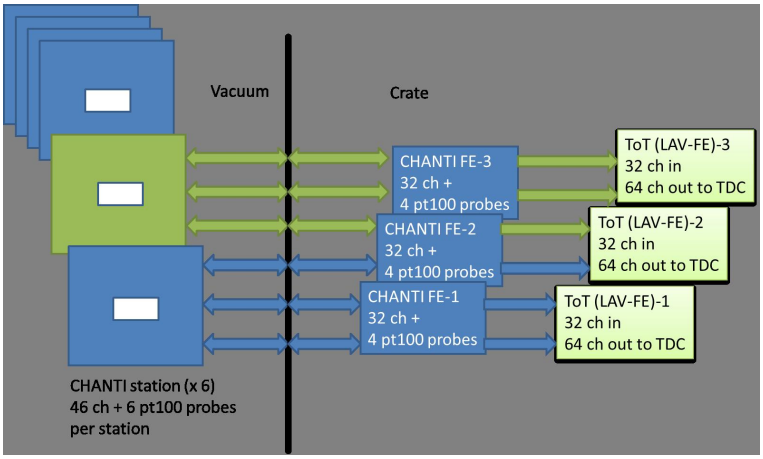


Figure 11: A schematic view of CHANTI two level FEE.

construction of the stations. This is indeed crucial since after one bar is glued inside a CHANTI station it cannot be replaced. Less than 2% of the manufactured bars have failed the validation test. The full procedure to assembly and cable one station has been already demonstrated for the prototype station used in the TR, including the operation of the station in vacuum and the use of the signal feed-throughs. The assembly of the six stations will begin in May 2014, and will last about one month. The full CHANTI hardware will be delivered to CERN by end of June 2014.

## 5.2 Front End Electronics

During the technical run a prototype board for the CHANTI FEE electronics chain has been tested and validated. The readout scheme for the CHANTI is a two level one, as shown in figure 11. The signals from each of the six stations are grouped on three SUB-D37 feed-throughs (16 ch each) and then fed to the CHANTI-FE boards. Each CHANTI-FE board can manage up to 32 channels. For each channel it is able to set the SiPM bias voltage (with mV resolution), to read its current (with nA resolution) and to amplify the signal (25 times amplification for 50 Ohm impedance). Each board can also monitor up to 4 Pt100 temperature probes, placed on the detector, in order to follow the temperature variations and compensate the response of the SiPMs.

The (analog) output from the CHANTI-FE board is digitized using the LAV-FE boards, which generates an output LVDS signal whose duration is the amount of time the input analog signal was above a given threshold (ToT). Two thresholds (referred to as High and Low thresholds) are available for each input channel, so that 32 physical channels are finally mapped into 64 TDC logical channels. The full electronics chain includes the standard TDCB+TEL62 readout system.

The LAV-FE boards have been already produced; the tender for the construction of all of the CHANTI-FE boards has been completed in January 2014 and the boards are expected to be delivered by end of March 2014.

## 5.3 Monte Carlo simulation

A complete description of a CHANTI bar, including all the optical interfaces between the scintillator, the glue, and the fibre (and inside the fiber itself), and including also a

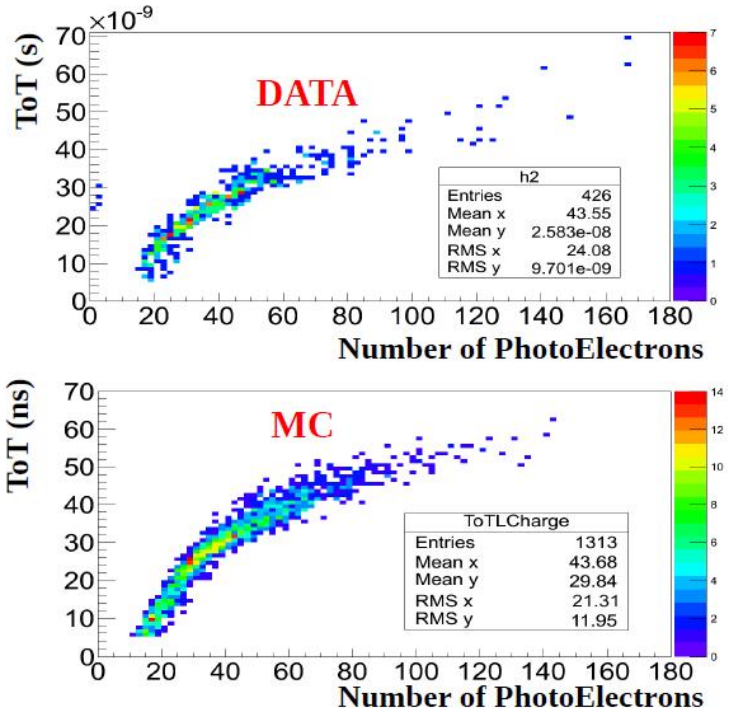


Figure 12: A DATA-MC comparison for the detailed simulation of a CHANTI bar. The simulation refers to a MIP, the data is from a cosmic ray tests, the threshold chosen is 80 mV.

detailed simulation of the photodetector and of its response has been carefully carried out. It turns out that such a simulation is able to reproduce all of the most relevant features of the measured signal. A figure of merit of this kind of simulation is the relation between the charge collected (in photoelectrons) and the ToT for different values of the threshold. A typical result of this comparison, is shown in figure 12 for a MIP (with the proper angular distribution simulated in order to reproduce cosmic rays data) at a threshold of 80 mV.

A work is currently in progress to include a parameterized (fast) version of the detailed simulation/digitization of the CHANTI inside the full GEANT4 simulation of the NA62 apparatus.

# 6 Straw Tracker

The Straw tracker consists of four stations, each made of two modules rotated by 45°. Each module consists of two perpendicular views and each view is made of four layers of straws. The production of the straw tubes has been completed in JINR (Dubna). About 400 spare straws will be delivered to CERN. Assembly of the Straw modules took place both at CERN (four modules) and at JINR. The assembly of the CERN modules is complete. In JINR three of the four module are complete and the production of the fourth has started. The UV (Ch2) was delivered to CERN in October 2013, while modules XY (Ch2) and UV (Ch4) are expected to arrive at CERN at the beginning of April. The module under construction is expected to be at CERN in June 2014.

In 2013 major progress was achieved on the Straw electronics. The production of the on-detector electronics housing the frontend, TDC and services was completed, all

modules were tested and they are being installed on the chambers. The specification and design of the final SRB (Straw Readout Board) is complete and the layout and schematics are soon to be launched.

Power supplies are being procured and patch panels, cabling and services to dress the chambers (Fig. 13) are in construction. The whole gas system was procured and is being installed.

Figure 13: The dressing of a Straw module

# 7 RICH

The RICH detector is needed to suppress the $\mu^+$ contamination in the $\pi^+$ sample by a factor of at least 100 in the 15 to 35 GeV/c momentum range, to measure the pion crossing time with a resolution of about 100 ps and to produce the L0 trigger for a charged track. The detector will consist of a 17 m long tank, filled with neon gas at atmospheric pressure, with a mosaic of 20 spherical mirrors with 17 m focal length, placed at the downstream end, and about 2000 photomultipliers (PMTs) placed at the upstream end.

The RICH vessel is a vacuum proof tank, made of construction steel, subdivided into four drums of decreasing diameter between 3.9 (upstream end) and 3.2 m, together with a truncated cone shaped part for the connection with the smaller diameter NA62 vacuum tank. The vessel was delivered to CERN at the end of January 2014 and its installation completed in March (Fig. 14). The RICH exit window is a refurbished NA48 Al window; the thin entrance window is new. An Al beam pipe will span the length of the RICH to keep the beam particles in vacuum; it is under fabrication with installation foreseen for the summer 2014.

The mirror mosaic is composed of 18 spherical mirrors of hexagonal shape (350 mm side) and two of semi-hexagonal shape to be located close to the beam pipe; all the mirrors have already been manufactured, their optical quality has been tested and they are at CERN since summer 2011. The aluminization of the mirrors is under way at CERN; the coating process will be completed by April 2014.

Figure 14: Left: two RICH vessel sections in the NA62 cavern. Right: the first section of the RICH vessel, with the conical cap and the entrance window already installed

An aluminum honeycomb panel will be placed in front of the exit window of the vessel to support the mirror mosaic; this panel, 50 mm thick and divided into two halves, was designed to be stiff enough for the 400 kg load of the mirror mosaic but at the same time as transparent as possible to photons to be seen by the downstream LKr calorimeter. The order for panel fabrication was submitted in December 2013 and the delivery is expected by the end of April 2014.

Each hexagonal mirror has a cylindrical hole, 12 mm wide, in its rear (i.e. not reflecting) surface, close to the geometric centre; an aluminum dowel, inserted into the hole and connected to the panel, will support the mirror. Two thin aluminum ribbons, attached at the mirror rear surface at about 200 mm from the hole, will keep the mirror in equilibrium and allow its orientation. The semi-hexagonal mirrors have two holes and a single ribbon. The mirror system installation is foreseen to start in May 2014 and to be completed by the summer. The mirror alignment system is based on piezo-motor actuators connected to the mirrors by thin aluminum ribbons: all the piezo-motors (two for each mirror), with their encoders, have been bought and will be mounted on the support panel in May 2014.

Pure neon gas will be injected into the vessel after vacuum has been established inside; a system of gas purification and recirculation is also considered as a backup solution. The neon filling is scheduled at the end of summer 2014.

About 2150 Hamamatsu R7400-U03 PMTs have been bought, delivered and tested, including 10% of spares. PMT HV-dividers are custom made. The first PMT lodging disk with 976 PMTs was completed in December 2013; the second disk will be completed by the end of March 2014. All the required HV power supplies have already been purchased and are available. HV distribution boards have been completed in December 2013. The installed PMTs will be fully tested with a laser set-up in a laboratory in Firenze before delivery to CERN. The PMTs readout electronics is also custom made and will be completed in spring 2014; the readout electronics, based on the NINO ASIC, has been extensively checked in two test beam runs with a RICH prototype and a new version is needed only to provide the proper channel multiplicity required by the NA62 DAQ system (each board has 32 channels; there will be 64 boards distributed over four crates). The installation of the PMTs lodging disks on the RICH vessel is scheduled for September 2014, together with the corresponding electronics; the DAQ system is based on five TEL62 boards (four for the 1952 PMTS, one for a multiplicity output from the front-end readout) of the same type used by other NA62 detectors.

The RICH schedule allows the full installation to be completed and the detector commissioned before the NA62 run foreseen to start in mid October 2014.

# 8 Photon Veto

The principal achievements of the Photon Veto team in 2013 were in the design and construction and commissioning of the LAV system , in particular progress was made on:

- Continued processing of lead-glass blocks for use in LAV stations A9, A10, A12 (structural reinforcement, cleaning, characterization, and testing);
- Assembly and transport to CERN of A9 and A10;
- Production of final drawings for station A12, which is operated in air and is thus of a different design from the other stations, tendering and assignment of the order;
- Installation of LAV 9 station on the NA62 beamline;
- Mass production and testing of the LAV frontend electronics boards;
- Cabling and HV test for LAV1-LAV5, commissioning of the electronics for the first 5 stations;
- Development of level-zero trigger firmware for the LAV system

The LAV system consists of 12 stations. The diameter of the stations increases with distance from the target, as does the number of blocks in each, from 160 to 256, for a total of about 2500 blocks. Each station consists of four or five rings of blocks, with the blocks staggered in azimuth in successive rings. The total depth of a five-layer station is 27 radiation lengths. This structure guarantees high efficiency, hermeticity, and uniformity of response.

Following the delivery of A7 to CERN in early 2012, stations A8 and A11 were constructed and delivered. A11 was the first station of large diameter to be completed and required the development of new technical solutions for aspects of the cabling and assembly. As of the end of 2013, eleven of the 12 stations have been completed and delivered to CERN. So far during the construction of the LAV detectors, more than 2500 lead-glass blocks from the OPAL electromagnetic calorimeter have been processed (structural reinforced, cleaned, characterized, and tested). The basic design of the A12 station was completed. In particular, the arrangement of the blocks, the mechanical structure, and the basic cabling scheme were all finalized. The design of the A12 station is different from that of the other 11 stations in many important aspects: it is operated in air rather than in vacuum, it is modular rather than monolithic because of its large size, and its installation into the confined space at the downstream end of the beamline will require a delicate insertion procedure.

In order to test and characterize the 100 LAV-FEEs, an automated test stand was set up at LNF . A pulse generator (Agilent 81110A) is used to generate test signals with a fixed rise time of 5 ns, a fall time of 16 ns, and variable amplitude. The signal is passively split into 32 copies and fed into the input DB37 connectors of a frontend board. The 64 LVDS outputs are connected to a VME commercial board (CAEN V1190B), which makes use of the same TDC ASIC as the actual TEL62 readout (HPTDC). The digital

data from the TDCs are collected through a VME controller (CAEN V1718) and stored on a PC. The PC additionally sets the threshold values on the frontend boards via USB, and varies the amplitude of the signals from the pulse generator via GPIB. The procedure is fully automated; a complete test of a frontend board takes about 15 minutes.

Plans for 2014 include2014:

- contruction and commissioning of LAV12;
- installation of LAV 10-12;
- cabling;
- FEE installation and commissioning of LAV A5-A12 to be ready for the data taking.

## 8.1 SAC and IRC

The SAC and IRC detectors are crucial for the vetoing of the particles, flying at small angles with respect to the beam direction. During this year the following tasks were accomplished:

**Detector construction**

In the data from the 2012 NA62 technical run the signals from the SAC detector were measured to have length of more than 30 ns FWHM. Moreover the photoelectric yield of the PMTs used during the prototype assembly and the NA62 technical run (FEU-85) was about an order of magnitude lower at their nominal operational voltage. This lead to the decision to change the PMTs to Hamamatsu R6427 ones which have fast rise time ($\approx$ 1.7 ns). The PMT mounting mechanics was updated accordingly and the determined photoelectric yield was consistent with that expected. The WLS fibers for the IRC detector were delivered to CERN after few wrong deliveries and are available at present. Concerning the scintillator a study of the possible geometrical solutions and tile manufacturer has been undertaken. It was decided to obtain 300 square tiles with side 150 mm and thickness of 1.5 mm and to perform the necessary cutting and drilling of the holes for the fibers afterwards. A study to identify a suitable scintillator was undertaken and after it ended an order has been placed. The scintillator was delivered to CERN at the end of August. In October it was painted with a white reflective paint to protect it from the lead in the assembled sandwich. The scintillator was sent to IHEP-Protvino for drilling and cutting. An unexpected delay occurred due to the necessity to match the holes of the already produced lead rings (punched using a pre-machined matrix) and the holes of the scintillator, planned to be drilled by a CNC. A series of measurements were undertaken to confirm that it was possible to match the holes in the lead with the holes of the original matrix and to produce a map of all the 570 holes, suitable for the CNC. This delay of $\approx$ four months at present is not crucial, but puts a tight constraint of the assembly activities. A decision was taken to complete the IRC assembly at the LNF-INFN. As result also the detector design was completely reviewed and assembly tools are in preparation.

**BTF test run**

The upgraded SAC took part in a test run at BTF-LNF from 24th till 30th of June, 2013, readout by digitizers. It was operated on a single electron beam with energy of $\approx$ 600 MeV. The SAC detector showed clear separation among the deposited energy of single, double and up to eight electrons, arriving in the 10 ns time window of the BTF beam. The linearity and the energy resolution were measured together with the

inefficiency of the detector for registration of 600 MeV electrons, which was lower than 5 $10^{-3}$ with indication that was as low as 6 $10^{-5}$. results are shown in Fig. 15.

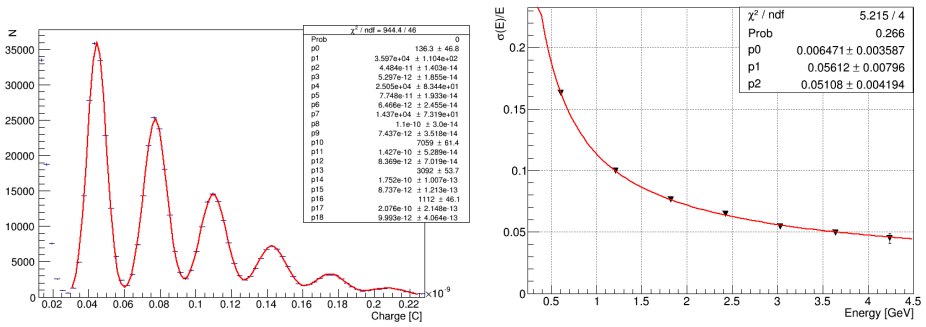


Figure 15: Charge measured by the SAC at the BTF test run (left) together with the obtained energy resolution (right)

Another issue during the test run was the operation and the performance of the possible solution of the SAC and IRC readout - the GANDALF framework with digitizer mezzanine boards. The GANDALF was operated in parallel to the CAEN V1751 digitizer and signals were recorded. After the BTF test run the SAC was transported back to CERN and is ready for reinstallation.

**Readout**

Due to the high expected rate and the necessity to be able to distinguish between beam halo muons (occurring randomly) and low energy electron and positrons from photon conversions (in time with the event) an ADC readout is a must for the IRC. The data chain and the readout model were defined and described. The necessary resources for the development of such a readout starting from zero for only four channels (eight, including the SAC) was realized to be not feasible and a commercially based design was adopted. The GANDALF framework (developed by Freiburg for the COMPASS experiment) was identified as viable solution after investigating more than five alternatives. It provides eight channels of 500 MS/s and an optical interface board able to sustain transfer of 3.1 GB/s. A version similar to the chosen readout (with 1 GS/s digitizers, decreased dynamic range and number of channels) was obtained in June and was tested both at he BTF test run and at the NA62 dry run. An updated version of its firmware was implemented and it was able to lock the clock and decode the trigger of the NA62 experiment, including the special Start-of-Burst and End-Of-Burst triggers and signals. This new firmware was able to sustain a rate up to about one MHz of NA62 triggers. At present a complete GANDALF module, serving both the SAC and the IRC and equipped with the final digitizers is available. The optical interface on the PC side (serving to record the data send from GANDALF) was ordered and is expected to arrive soon.

**Current Activities**

The major tasks towards the completion of the small angle photon veto system are the following:

- drilling the scintillators: time scale - end of March;
- assembly of the IRC detector: two months foreseen, April-May;
- transport to CERN: June;

- integration in the NA62 setup: July - August;
- readout: ongoing tests and development on the data transmission part of the GANDALF firmware by the GANDALF developers.

# 9 CHOD

The NA62 experimental apparatus includes a fast scintillator system, called Charged Hodoscope (CHOD), to detect tracks with precise measurements of the arrival time and impact point, to provide a fast signal to drive the trigger and data aquisition (TDAQ) system and to suppress background signals when used in anti-coincidence. The CHOD consists of two planes of 64 vertical and 64 horizontal BC408 plastic scintillator counters, each one read by a Photonis XP2262B photomultiplier (PM). The counters are assembled into 4 quadrants per plane, installed upstream of the LKr calorimeter. New front-end and read-out electronics has been provided to the CHOD, relying on systems already developed within NA62. The front-end electronics used for the Large Angle Veto (LAV FEE), consisting of Time-over-Threshold (ToT) discriminators with double threshold setting availability, is suitable for the CHOD. One TEL62 board with two TDCB, and four LAV FEE modules are needed. A HV system based on SY403 mainframes, used in NA48 and still working, will power the CHOD PMs in 2014. A track signal in the CHOD is given by the coincidence between one vertical and one horizontal counter of adjoining quadrants. The firmware for this trigger logic will be implemented within the TEL62 FPGA and used to select one or more tracks at the L0 trigger. The coincidence signal will also define the position of the track impinging the CHOD and will allow the hit time to be corrected taking into account the impact point on the detector. This correction will be implemented online, within the TEL62 FPGA. The use of ToT frontend will allow a rough online correction of the time of small signals due to slewing effect.

# 10 LKr

During the spring of 2013, the old readout has been dismounted: the crates and modules have been prepared for storage and/or disposal, all the cables were cut and the racks were completely emptied. New VME crates and PC to VME bridges have been delivered by CAEN. Almost all the new crates were temporarily installed in empty racks, connected to the power distribution and left switched on for several months in order to spot early defects in the power supplies or fan trays. At the same time, the crates were integrated in the experiment DCS and tested.

The power distribution and the cooling system of the readout racks have been redone completely, both to have new infrastructure and to free as much space as possible in the racks to be able to install network switches and optical splitters on the back of them. The cooling work has been completed early 2014.

The layout of the racks has been studied and optimized to have the cleanest cable passage on the front and to leave as much free space as possible for the passage of the cooling air.

The clock distribution modules for the CREAM crates has been produced and tested. The special P0 backplanes to distribute the clock to the CREAM modules have been produced and tested.

During the dismounting of the old readout system, a check was made on all the input signals, using the calibration pulser and looking with an oscilloscope at the signal to be sent to the CREAM inputs. This was performed to spot possible problems in the electronics upstream of the readout (i.e. transceiver faults, bad signals from preamplifiers, etc.).

## 10.1 CREAM modules

CAEN has delivered a first pre-series of 16 CREAM modules (Fig. 16) in October 2013. Since then, they have been installed in a dedicated crate in the experimental area and connected to a network switch with a 10 Gb uplink to the NA62 PC farm.

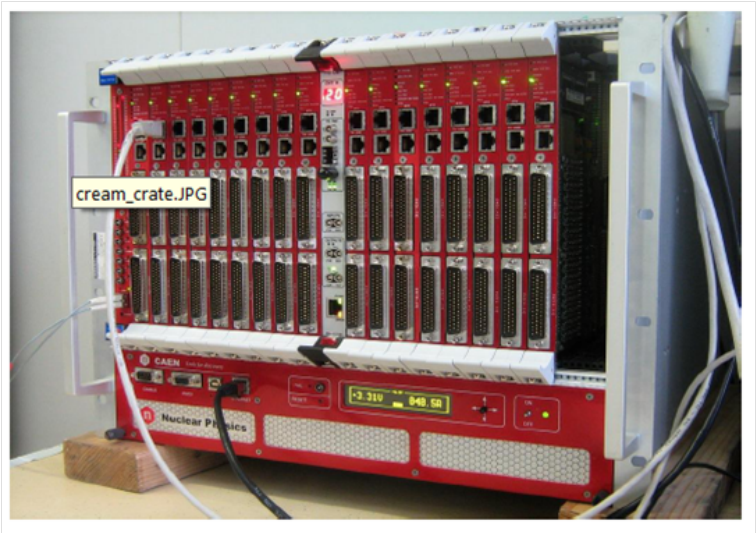


Figure 16: Pre-series of the CREAM modules delivered by CAEN

A series of tests have been performed with the NA62 PC farm; the complete chain foreseen for the experiment has been used: periodic L0 triggers are sent to a TEL 62, whose data are then transmitted to the PC-farm. The PC farm generates a L1 request to the CREAM modules every L0 input packet, data from the CREAMs are then sent to the PCfarm and the event is built and then written on disk.

Both pedestal and calibration data have been collected. Pedestal data have been used to measure the noise of the system, as shown in Fig. 17: here the distribution of the pedestals of channel #0 of all the 16 CREAMs is shown and the wider distribution (the violet one) is related to the channel which was connected to the front-end electronics, while the others had their inputs open.

Calibration pulses are shown in Fig. 18 and Fig. 19: the second one shows the evolution of the undershoot of the calibration signals with an acquisition of 128 samples per event.

A continuous test activity, started in 2013 and still continuing, aims at testing the data transfer protocols between the CREAM system and the PC farm. With these tests we have tuned the firmware of the CREAMs, spotting bugs and getting a prompt response from CAEN. We have also done a significant debugging of the PC farm software, to be able to reach the 100 KHz L1 requests to the CREAM that we want to achieve.

At the end of February 2014, CAEN has delivered the first 11 modules of the final production: the testing rate in CAEN is around 40-50 modules/week, the deliveries will

be every two-three weeks, so that by middle June all the modules should be available for the installation.

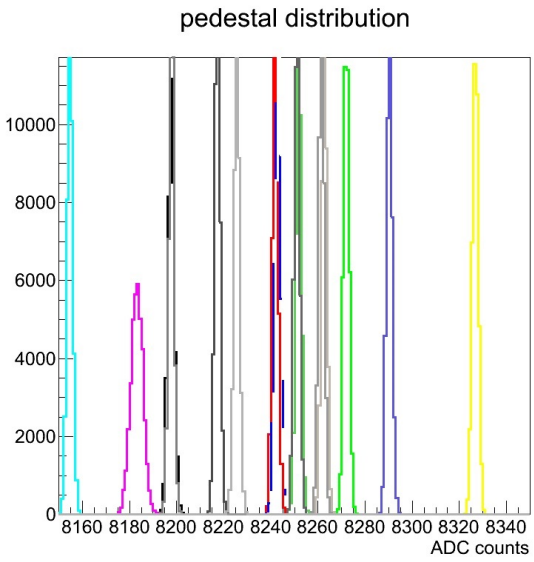


Figure 17: Pedestal distributions for ch 0 in 16 CREAMs

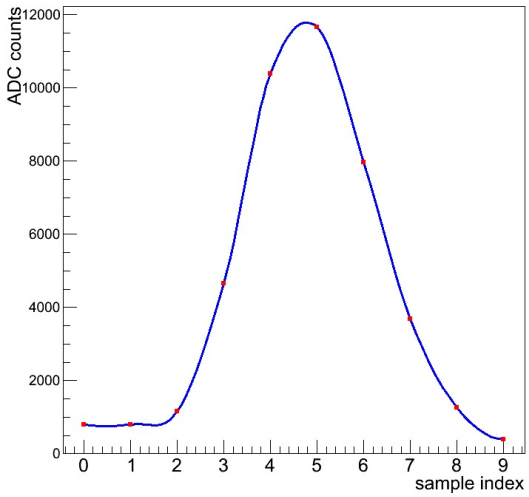


Figure 18: A typical calibration pulse, taken with 10 samples

# 11 Muon Veto System (MUV)

The Muon Veto detector (MUV) is essential to suppress kaon decays with muons in the final state. It consists of three independent modules, following the LKr and called MUV1, MUV2, and MUV3 in the order of their longitudinal position (Fig. 20). While MUV1 and MUV2 are iron scintillator sandwich calorimeters, the MUV3 detector consists of thick scintillator tiles for fast and efficient muon suppression at the trigger level.

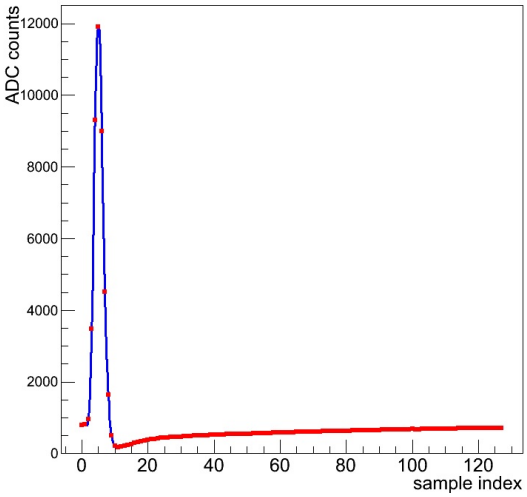


Figure 19: A calibration pulse, taken with 128 samples

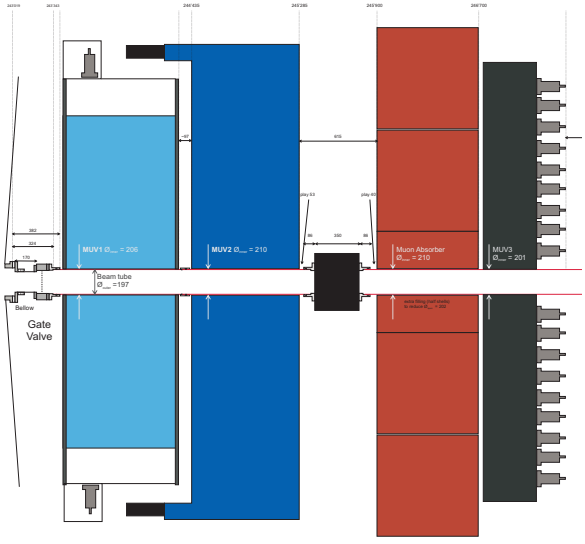


Figure 20: General set-up of the three muon veto detectors MUV1, MUV2, and MUV3

## 11.1 MUV1 Detector

The MUV1 module is made of 25 iron and 24 scintillating layers with in total almost 1100 scintillating strips. The strips are read-out with wavelength-shifting (WLS) fibres on both ends. The scintillators were produced by the Protvino group in 2012. However, since several strips did not match the requirements an additional production of about 250 strips is currently on-going.

In Mainz, the scintillators are further processed: each strip is diamond polished and two grooves for the WLS fibres are made. The grooves are filled with optical glue and the fibres are put in place. After measuring the performance in terms of light yield, each strip is wrapped in aluminized Mylar foil and made ready for the final assembly. A good fraction of the strips have been made ready for the installation in 2013. In addition, an LED calibration system has been developed and constructed: Each scintillating strip is equipped with an LED with 400 nm wavelength. The LEDs of different scintillating layers can be controlled independently for being able to calibrate single strips.

The final MUV1 construction is ongoing at the University of Mainz and is planned to be finished in early summer 2014. Immediately after the detector will be shipped to CERN and installed in the NA62 beamline.

## 11.2 MUV2 Detector

The MUV2 detector — the former NA48 hadron calorimeter (HAC) front module — was already fully operational in the technical run end of 2012. In 2013, only some remaining light leaks were fixed which had caused noisy channels during the technical run.

## 11.3 MUV3 Detector

The fast muon veto detector (MUV3) was constructed in 2011 and the beginning of 2012. It consists of scintillating tiles of $22 \times 22$ cm$^2$ cross-section and 5 cm thickness, produced at IHEP (Protvino). On the backside, each tile is simultaneously read out by two PMTs. As the MUV2 detector, the MUV3 was already operated during the technical run 2012 with 135 of 148 tiles being equipped with PMTs.

In 2013, additional 60 EMI 9814 PMTs were recuperated from the CDF experiment. These were used to equip the remaining tiles and to replace about half of the Philips XP2262 PMTs, which have different timing characteristics. The remaining tiles with Philips PMTs are now all on the corners of the MUV3 detectors. Furthermore, additional PMT bases (recovered from the CDF experiment) were installed.

In 2014, the old NA48 AKL constant fraction discriminator (CFD) boards will be replaced by new CFD boards which are developed and produced in Mainz. They will allow direct connection to the TDCB boards and will also have coincidence outputs for the two PMTs of the same tile.

# 12 Trigger and Data Acquisition

The development of the TDAQ system saw very significant progress in several different areas, with a noticeable speed-up in most of the work during the past year. The activities were paced by two more coordinated "dry runs" taking place at CERN in July

and November 2013, which followed those in 2012 and focused on the shortcomings experienced there; these confirmed to be highly beneficial to advance the development and integration. One of the things learnt from the tests was the need for implementing more complex and realistic laboratory test setups, in order to identify and solve issues which only appeared in run-like conditions at CERN. As foreseen, no trigger generation could be tested in 2013.

The **common system** developed in Pisa to be used by CEDAR, CHANTI, RICH, CHOD, LAV, MUV3 and partly by the LKr L0 trigger is well advanced. The TDC daughter-cards saw no need for further hardware development. Some fixes in the firmware were implemented to address a few issues observed in the data collected during the technical run of end 2012. All cables have been bought, and the boards themselves are ready for full production which is expected to start in March 2014 (100 boards out of 125 still to be built).

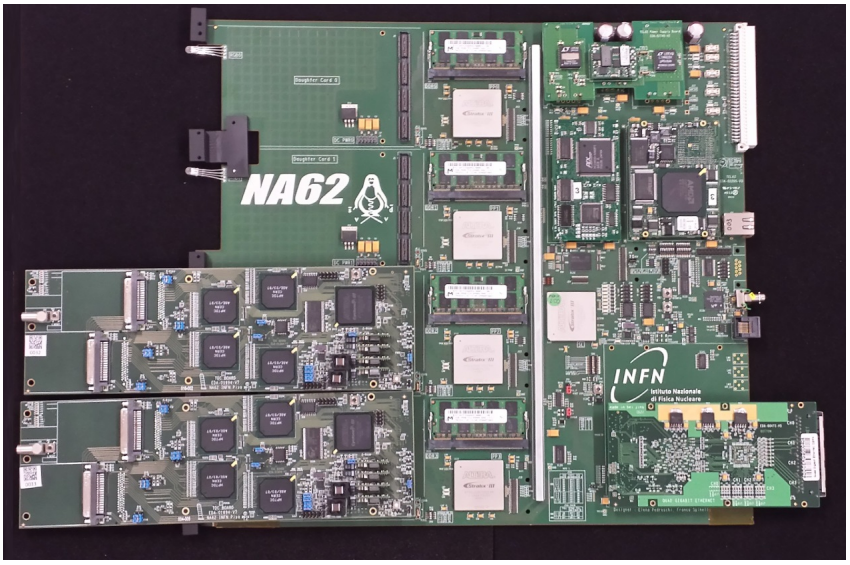


Figure 21: The V3 TEL62 board with larger FPGAs and power-distribution daughter-card and two TDCB plugged in

The main TEL62 board (Fig. 21) saw a significant development in the firmware, with the goal of surpassing the rate limitations experienced during the 2012 technical run, which focused on the readout branch. Specifically, the whole scheme for event data storage in memory during the 1ms L0 trigger latency was completely rewritten in a highly optimized way: this allowed to gain an order of magnitude in the sustainable trigger rate, from 100 kHz in 2012 to the design value of 1 MHz in 2013. This success finally resulted in the validation of the concept, and also confirmed that the hardware concept of the board requires no significant change: indeed the layout of the final version V3 only differs in minor details from the original one, the most significant being the implementation of a small power distribution sub-card to allow easy replacement and modification. Significant contributions to the coding of the sub-detector firmware (for monitoring and L0 triggering) came from sub-detector groups: the TEL62 L0 trigger firmware for the LAV was written, simulated and tested by the Frascati group, and is now complete as far as triggering from a single LAV ring is concerned; the TEL62 L0 trigger firmware for the RICH was also written and simulated and is being deployed and tested on the hardware by the Perugia group, which also started doing the same for the charged hodoscope (CHOD).

Having some of the sub-detector firmware available in hand, it was realized that the amount of available resources in the FPGAs on the TEL62, while adequate, would not have allowed comfortable increases in firmware complexity, which could be reasonably expected during the lifetime of the experiment, without sacrificing the extensive deployment of debugging features which were found to be instrumental in understanding the behaviour of such a complex system. The proposal was made to **upgrade** the board to a pin-compatible FPGA with roughly twice the amount of resources, an option which was kept open in the original design. This was recommended by the collaboration, and in September 2013 extra funding was secured from INFN (which concerns 85% of the boards), and the acquisition of the new devices was started. In order to overcome the manufacturing shortcomings experienced on the first TEL62 prototypes, a new production firm was identified and five prototypes (of the final version with the larger FPGAs) were produced: still a few manufacturing defects were found on two of those, both due to bad soldering, which could be solved easily and indicate the need for a re-tuning of the procedure at the mounting firm. The upgrade somewhat delayed the foreseen board production schedule: full production (78 boards out of a total of 83 for NA62, to be produced in at least 2 batches; 11 more boards are going to be acquired by some LHCb groups for testing upgrade projects) is now ready to start, waiting for the availability of FPGAs. Unfortunately, delays with order placement for the new FPGAs in Rome Tor Vergata imply the first batch of devices will only be available by the end of March 2014, setting the schedule for board production, which is however still expected to be in time for the run, although some issues with board testing might arise. Concerning board testing, a semi-automated test procedure was set up by the Roma Tor Vergata group, which allows a quick assessment of hardware failures on the boards as they are received from the firm. Radiation tests on the TEL62 were performed by the Birmingham group: while these were only partially realistic, no issues were found, and more tests are scheduled.

The **L0 trigger generation** system for LAV, RICH, CHOD and MUV3 remains to be tested, although for at least the first of these detectors significant laboratory tests could be performed, successfully showing the dispatching of L0 trigger primitives over ethernet. A missing part is the intercommunication between different TEL62 boards, essential for those sub-detectors which are spread over more than a single board (RICH and LAV): the Perugia group started working on this during the summer, producing the design of a small serial interconnection daughter-card which is now ready for prototype manufacturing; firmware development for this element is expected to start soon in Perugia and Frascati, and will require sub-detector groups involvement for specific parts.

The **L0 trigger system for the LKr calorimeter** is massively based on TEL62 boards, although with a different firmware, and with the addition of three kinds of intercommunication boards. Such boards were developed in Roma Tor Vergata with the participation of the Perugia group, and prototypes were successfully tested both in the laboratory and at CERN together with the first prototypes of the CREAM calorimeter readout modules. Pre-production batches are expected to be available in the beginning of June, and the full production at the end of July, in a very tight schedule. Firmware development progressed nicely, obtaining a detailed implementation which allowed a realistic assessment of the required resources and latencies: the new larger FPGAs allowed a significant simplification in that calorimeter trigger data can now be stored in the internal memory, thus not requiring the use of the external memory, and the latency was determined to be close to 11 $\mu$s in normal conditions.

The status of the readout for the detectors which do not use the common system

is also described in the corresponding sub-detector sections, so only brief information is given here. The **LKr calorimeter** is going to be read with the new CREAM flash digitizers developed by CAEN for NA62: the pre-production modules were successfully tested both in a standalone mode and together with the prototype L0 trigger receiver board and the green light for the full production was given. The system is expected to be fully installed for the 2014 run.

The development of the **Gigatracker** off-detector readout electronics saw good progress: in 2013 the firmware was upgraded, focusing on the complex external memory controller and the implementation of data emulators for the TDCpix chip. During the November 2013 dry run at CERN emulated data was sent to the prototype readout boards (Fig. 22), extracted following simulated L0 triggers received through the standard TTC link, formatted and sent to a readout PC. The full production of 35 motherboards was launched, and the design of the timing daughter-cards was finalized and prototype production started.

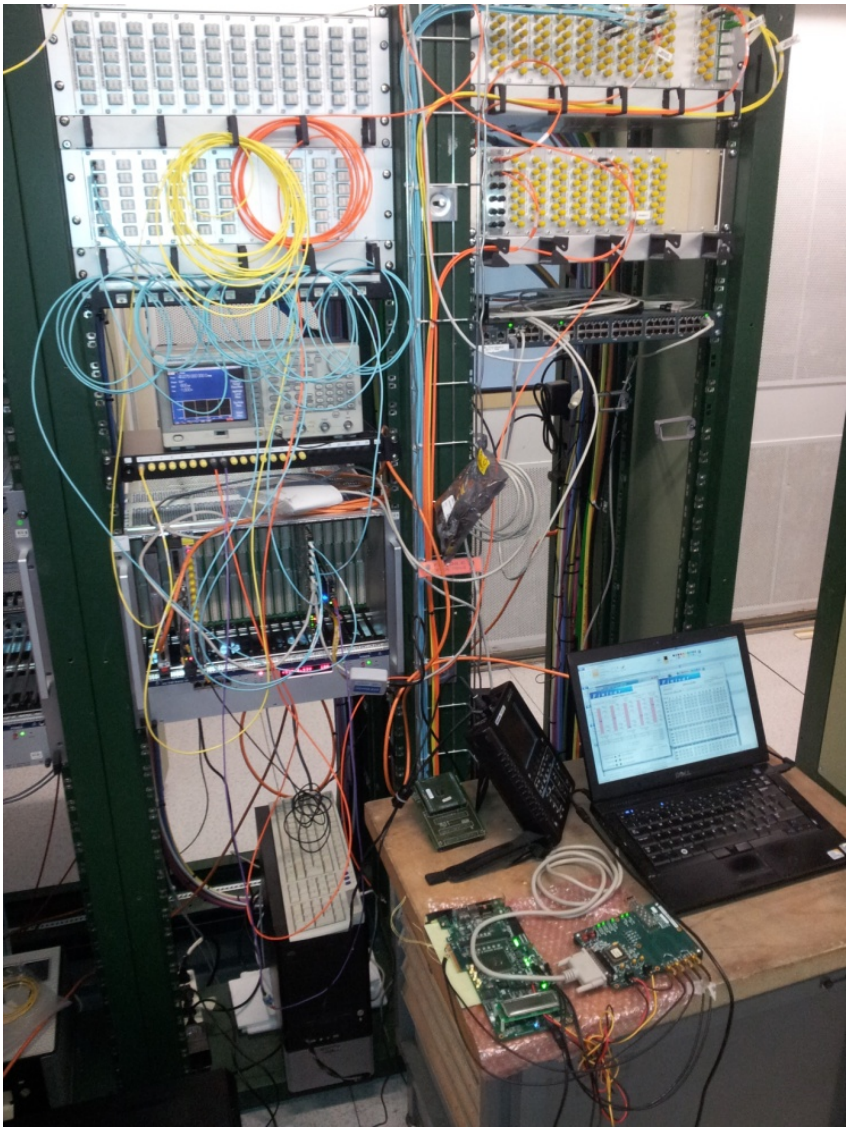

Figure 22: The GTK test readout setup during the November 2013 dry run

For the readout of the **SAC and IRC** detectors, a realistic scheme was identified, based on a customized version of the COMPASS Gandalf readout board using high-speed

digitizers, for which a collaboration with the development team was established. The prototype system is available and requires some firmware changes expected in spring; installation at CERN is expected to happen in July 2014. For the **Straw** system the full production and testing of 540 front-end boards was completed, and the effort is now focusing on the development of the final SRB readout board to handle event management, selection and formatting: prototype SRBs are expected to be available in May 2014, so that the production modules can start before the summer.

The central **L0 Trigger Processor (L0TP)** project has seen the participation of a new very experienced group (Torino). The strengthened team is now evaluating two versions of the L0TP, a PC-based version and a fully-FPGA one. These two options share most of the underlying infrastructure (e.g. the ethernet receiver firmware developed in Ferrara, the hardware TTC interface board developed in Torino) and data transmission tests were carried out at CERN in November 2013 using simulated data from TEL62 boards for both systems. The necessary hardware for both versions has already been procured. The choice will be based on the flexibility in handling more L0 trigger conditions. For lower rate applications and tests the TALK board, employed during the 2012 technical run, remains a viable option. Concerning the **general infrastructure**, the deployment of the network interconnection system in the experimental area was completed. Some puzzling issues related to early hardware failures on NA62 crates could not be understood completely: while some failures were eventually acknowledged as manufacturer's faults, for others no viable explanation was found; the experiment and procurement schedule forced NA62 to order all crates nevertheless, and a monitoring plan is being implemented to immediately spot further similar failures, should they occur. The origin of these faults continues to be investigated. The interface of several systems with the **DCS and the Run Control** was tested: such systems are quite advanced. A scheme was finalized in an internal note for the handling of configuration files and sub-detector initialization, as well as for the interface to the online database where such information must be stored; common software was developed to allow a uniform approach throughout NA62, which is scheduled to be tested at CERN in spring. Summarizing, a lot of progress was made during the past year, with major steps forwards in some systems and a positive trend. A TDAQ commissioner has been appointed in order to keep up with a tight schedule of coordinated tests in view of the scheduled beam run in the fall.

# 13 Publications and analysis of older data

Since the last SPSC review in April 2013, three physics analyses have been completed, based on older data recorded in 2003-2004 (NA48/2) and 2007 (NA62). The NA48/2 collaboration has completed the analysis of a small sample of $K^{\pm} \to \pi^{\pm}\gamma\gamma$ decays (BR of $O(10^{-6})$ published recently [6]. Another analysis of a rare decay mode $K^{\pm} \to \pi^0\pi^0 e^{\pm}\nu$ (BR of $O(10^{-5})$ but still poorly known) brings precise measurements of both decay rate and form factor. A draft paper is currently under review within the Collaboration [7].

The NA62 collaboration has taken advantage of a sample of minimum bias triggers collected concurrently with the main analysis trigger ($R_K$ measurement, already published in 2013 [8]). It allowed the measurement of another sample of $K^{\pm} \to \pi^{\pm}\gamma\gamma$ decays and its combination with the NA48/2 results. Chiral Perturbation Theory predictions of both decay rate and diphoton spectrum were validated and characteristic parameters were obtained. This latest publication has just been accepted by Phys. Lett. B [9].

More analyses of both NA62 and NA48/2 data are still on-going: the high quality data recorded in former years are still valuable either to explore poorly known very rare kaon decays or to conduct high precision measurements. They are also an ideal practice for Master and PhD students, working on hardware-related subjects, as a training fordata analysis.

The above topics include:

- a measurement of the structure dependent component of the radiative $K^{\pm} \to e^{\pm}\nu\gamma$ decay;
- a measurement of the $\pi^0$ transition form factor (from a sample of $K^{\pm} \to \pi^{\pm}\pi^0_D$ with Dalitz decay);
- a search for long-lived sterile heavy neutrinos $\nu_H$ in the $50 - 350$ MeV/$c^2$ mass range produced in the $K^{\pm} \to \mu^{\pm}\nu_H$ decay;
- a precision study of $K^{\pm} \to \pi^0 l^{\pm}\nu$ form factors in both $K_{e3}$ and $K_{\mu 3}$ modes;
- a first observation of the $K^{\pm} \to \pi^{\pm}\pi^0 e^+ e^-$ decay.

The collaboration is actively contributing to major International Conferences and topical Workshops with NA62 Detector contributions and recently published or preliminary physics results from NA62 and NA48/2 data analyses. In the past year (April 2013 to April 2014), the collaboration speakers presented 42 talks and three posters to Physics Conferences and 18 talks and 11 posters to Instrumentation Conferences. More contributions are foreseen in future 2014 Conferences.

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