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From TELL1 to TEL62

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Introduction

Since some years, the NA62 TDAQ group identified the general-purpose trigger and data acquisition board TELL1 (Trigger Electronics for Level 1) as a possible base solution for the readout and Level 0 trigger of several sub-detectors. The choice of an existing and common board has several advantages in terms of development time, debugging time, maintenance and handling of spares.

The TELL1 board [1] was designed at EPFL Lausanne for the LHCb experiment several years ago (project start around 2001), choosing what were state of the art components at that time. The approval and construction schedule of NA62 did not to allow the possibility of joining the last production of LHCb boards before LHC start-up (2008), so that the manufacturing of new boards will have to be taken care of within the NA62 collaboration. While the basic functionality of the board matches the needs of NA62, a critical evaluation of the board's features and components revealed that some of such devices are now becoming obsolete. In the long-term perspective of use within NA62 on a time scale which might extend to the order of 10 years, a partial redesign of the board was considered to be necessary.

The most relevant components of the boards are FPGAs and external buffer memories used for data storage during the L0 trigger latency. In the original TELL1 board the former belong to the Altera™ Stratix I family, and the latter are DDR dynamic memory chips directly soldered on the board; the most recent family of Altera™ FPGAs is now the Stratix V family (Stratix III being the one of most widespread use), and laptop PCs nowadays start using DDR3 memories.

The main update that we propose is to use newer FPGAs, with significantly higher logic element counts and larger internal memories, and to replace the external DDR memory (256 Mbit) with a much larger and faster DDR2 memory (2 GB or 4 GB socketed memory). These choices are dictated not only by the improvements which they can provide in terms of the board's capabilities, but also by cost and maintenance issues: the obsolescence of the FPGAs and memories limit their

availability with a corresponding price increase at a quick pace, as it happens in the fast-moving field of electronic components.

At the design level we propose to keep the same "star" (or "tree") overall structure of the TELL1 internal data flow, in which four FPGAs (PP-FPGAs) are devoted to the four daughter-boards (mezzanine cards) which can be housed on the mother-board, and a fifth one (SL-FPGA) merges and collects the data from the former, also handling its transmission to the outside.

Actually, one design choice was to keep the new board (nicknamed TEL62, Trigger Electronics for NA62) mechanically and electrically compatible with the TELL1, and therefore also able to house the LHCb daughter-cards, besides the new TDC daughter card designed for NA62. A few important modifications are however proposed, which will make the TEL62 board more suited to the use within NA62; such modifications are also described below.

Main design modifications

In the TELL1 each PP-FPGA is connected to the SL-FPGA through a single dedicated 32-bit bus (plus control lines). In the TEL62 each PP-FPGA will be connected to the SL-FPGA through two independent 32-bit buses (plus control lines). This allows having separate and independent paths for L0 Trigger primitives (where needed) and readout data streams respectively, avoiding the necessity of a logic arbiter and doubling at the same time the available bandwidth.

The TELL1 has an on-board connector called FEM (Front End Emulator) with 8 data lines (plus control lines). The corresponding functionality for which this connector is used in LHCb is not required in NA62, but at the same time there are plans to connect several TEL62 boards in a daisy chain through fast links, for the purpose of sharing L0 trigger primitive informations (e.g. for the RICH or the LAV). While such inter-board connection could be implemented by using two of the four Gigabit Ethernet links (fully implementing GbE receiver firmware and not using such two links for readout, therefore halving the output data bandwidth), we foresee on the TEL62 a new on-board connector (named AuxBrd), housing two independent 16-bit buses (plus control lines). Such a connector would allow an expansion of the board capabilities, e.g. the possibility of installing a new mezzanine card (still to be developed), which could house two fast serializers and the corresponding drivers and be used for inter-board communication. All the AuxBrd connector lines connect to the SL-FPGA, and therefore they could be used in any desired way by just changing the firmware.

The TELL1 board defined many clock distribution and return lines at the hardware level, to automatically synchronize the FPGAs PLL clocks keeping into account the line delays on the PCB. Such a feature was actually never used in the TELL1 firmware, and is removed in the TEL62, simplifying the design in this respect.

As mentioned, the FPGAs will be replaced with devices of the newer Altera™ Stratix III family. On the TELL1 the single SL-FPGA was an EP1S25F1020C7 (25K logic elements), and the four PP-FPGAs were EP1S25F780C7 (25K logic elements). The most natural replacement device for PP-FPGAs would be EP3SL50F780C4N (50K logic elements); unfortunately such device, despite the same total pin count as the original one, provides about 100 I/O pins less: while this is not a problem *per se* (not all I/O pins being used), the pin assignment constraints for maintaining compatibility with the LHCb TELL1 mezzanine cards (different cards work on different voltages)

suggest the use of a device with a larger pin count, which turns out to be the same one chosen for the new SL-FPGA. After considering the decreasing price, it was chosen to have all five FPGAs on the TEL62 (both PP-FPGAs and SL-FPGA) of the same type EP3SL110F1152C4N (110K logic elements). This newer devices has 4 times the logic, 2 times the internal static RAM, 2 times the speed with respect to the original one used for the SL-FPGA; moreover it has 4 times the number of internal PLLs and much lower "normalized" power consumption. The increased pin availability for the PP-FPGAs suggested the introduction of two 16-bit uni-directional communication buses between each FPGA and the neighbouring ones (4 buses per FPGA); the buses to/from the first and last PP-FPGA are connected to pins on the AuxBrd connector, where they can be connected to fully close the communication ring. This inter-communication feature among PP-FPGAs can be exploited by some applications (e.g. the electromagnetic calorimeter trigger system in NA62 LKr/L0). All pins in the PP-FPGA and SL-FPGA were allocated, and a Quartus™ design with all the pins assigned to proper locations was defined, in order to minimize PCB routing efforts. The Quartus™ design saturates almost completely the available pins for both PP-FPGAs and SL-FPGA.

As in the present TELL1 design, the four PP-FPGAs will be loaded with the same firmware, and the SL-FPGA with a different one, but a different flash memory configuration will be used in the TEL62. The single EPC16 configuration device will be replaced by two EPCS64 devices: one will configure the four PP-FPGAs (with the same firmware), and the other one will configure the SL-FPGA. Altera™ provides a master/slave scheme to configure several FPGAs as a clone of a single FPGA defined as the master. The EPCS64 devices are quite cheap but do not support a JTAG interface (while EPC16 does) so an additional small programming connector is foreseen for each flash memory. Altera™ however provides a logic cell to add "software" JTAG capabilities to the EPCS64 devices, by using the JTAG interface of the FPGA to be programmed. Such a scheme was successfully used on the TDC daughter board, which also houses an Altera™ FPGA.

In the TELL1 each PP-FPGA has an external buffer memory composed of three DDR-266 memory chips, for a total amount of memory of 16M x 48bit. Within NA62 these memories will be used to store the data waiting for the L0 trigger decision, and their size (together with the sub-detector event size) determine the maximum allowed L0 trigger latency. Obsolete soldered DDR memory chips will be replaced with a DDR2 Small Outline DIMM (SO-DIMM) socket, of the type used in notebook computers. Such socket can host memory modules up to 4 Gbytes, organized as blocks of 256M x 64bit. DDR2 have a maximum clock speed of 800 MHz, but the chosen FPGAs (speed grade 4) only support up to 667 MHz. The choice of having memories on sockets allows much easier replacement and upgrades. As an initial choice we propose to insert in the sockets the MT16HTF25664HZ-800C1 module (2Gbytes).

The QDR external buffer memory connected to the SL-FPGA will not be changed with respect to the TELL1.

Power

The voltages required on the TEL62 backplane connector will be the same as for the TELL1: +5V, +3.3V, +48V, +A5V, -A5V (the last two being "analog" voltages), with the same backplane connector configuration. The effort towards the definition of a common crate format for NA62 led to the suggestion of a 9U crate with power-only J3 backplane compatible with the TELL1/TEL62,

and the optional addition of +12V and -12V power and Analog Ground on some of the backplane pins not used by such boards.

Mostly due to the change of FPGA family and memories, the voltages generated internally in the TEL62 board are however quite different with respect to the TELL1. TELL1 internal voltages are: 1.5V, 2.5V, 3.3V, 5V, A5V and -A5V. The low voltages 1.5V and 2.5V are generated on the motherboard using PWM power supplies (DATEL UHE-1.5/100000-D48 and UHE-2.5/100000-D48) from the 48V voltage supply from the backplane connector; such devices work typically at 85% efficiency. The 5V and 3.3V are distributed from the backplane connector. Separated from the digital supplies, the "analog" +5V and -5V and the "analog" ground are also distributed from the power backplane.

The TEL62 has the following power requirements. Stratix III devices require 1.1 V to power the logic core; the FPGA PLL needs 2.5 V. The DDR2 RAM is powered to 1.8 V. In order to reduce the power supply requirements, and to gain a better noise immunity, many internal signals (between PP-FPGA and SL-FPGA) are defined as LVTTL 1.8V, therefore many FPGA blocks use 1.8V as VCCIO. The QDR (same model as in the TELL1) is now powered at 1.8V. The DDR2 SSTL signals require a parallel termination at VDDR2/ 2 = 0.9V (tracking of the 1.8V is required).

The 1.1V, 1.8V, 2.5V voltages will be generated internally to the TEL62 board using DC/DC converters working from the 48V supply (to gain better efficiency). Special care is needed to power the FPGA PLLs and the CERN QPLL device, in order to limit the clock jitter as much as possible (this is a major requirement for NA62, because clock jitter directly affects the resolution of the TDCs). We measured some jitter on the clocks generated by the TELL1 PLLs. To limit clock jitter, Altera™ application notes suggest to power each PLL analog power through its own (linear) power supply, and to add ferrite beads on the lines. The QPLL datasheet also suggest the use of a dedicated 2.5V power supply.

We call "global powers" the voltages used everywhere on the TEL62 board and distributed through PCB internal planes, while the voltages generated locally for a specific task are called "local". All local voltages require low power and low noise, so are generated using LDO linear converters.

DC/DC converters used for global power:

- PT4412A: 100Watt, 48V Input, 1.1V Output. It is an isolated DC/DC Converter provided by Texas Instruments™, with 86.5% efficiency.
- LQS100A48-1V8: 100A, 48V Input, 1.8V Output. It is a DC/DC Converter provided by Artesyn™ with 89.5% efficiency; a 50A version is also available in the same footprint.
- 0RSB-30T02L: 25 Watt, 48V Input, 2.5V Output. It is an isolated DC/DC Converter provided by BEL Power Product™, with 89% efficiency.

Regulators used for local power:

- 0.9V (DDR2 and QDR reference voltage) is generated on the motherboard by the TPS51100 Linear Regulator (by Texas Instruments™) using as input the 1.8V global power (4 devices needed, one for each SO-DIMM).

- 1.1V (FPGA PLL analog voltage) is generated on the motherboard by the LTC3026 Linear Regulator (by Linear Technology™) using as input the 1.8V global power (5 devices needed, one for each FPGA).

- 2.5V (QPLL voltage) is generated on the motherboard by the LM1117 800mA Low-Dropout Linear Regulator (by National Semiconductors™), using as input the A5V distributed from the crate backplane.

Following the original TELL1 design, the backplane power voltages 3.3V and 5V (digital) are used and distributed to the mezzanine connectors, and kept separated from the 5VA and -5VA "analog" voltages (not used by the TEL62 but only distributed to the mezzanine cards).

Due to the above changes in the power distribution scheme, and the use of different mezzanine cards in NA62, it is difficult to evaluate on paper the total power consumption required from the crate which will house the TEL62 boards; for what concerns the TEL62 board itself, an increased consumption on the 48V supply and a reduced one on the 3.3V can be foreseen. We note however that issues with the crate supply power requirements only concern crates housing large number of TEL62 boards; at present, within NA62, this is only relevant for the LKr/L0 trigger system, since the TEL62 equipped with TDC mezzanine cards occupies two slots of crate space.

Other minor modifications

External micro-switches will be added to program the QPLL lock frequency and operating mode. A mounting hole for a new communication card replacing the quad GbE card will be added (requested by A. Salamon). The RJ11 connector Molex™ 95001-2441, for the *choke/error* signals, will be replaced with 95501-2441 (requested by M. Krivda).

The current TELL1 relies on the crate reset power-on to reset all the FPGAs, while the CCPC is reset through a supervisor component. An additional Texas Instruments™ power supply supervisor TL7700 device will be added, to ensure the power-on reset status of all the logic, even if the board is not plugged in a crate.

Other components will not be changed: in particular the Credit-Card PC (CCPC) and the custom-built "Glue card" will be the same as in the TELL1, as well as the quad-Gigabit Ethernet card; the first two are available, while the third will have to be manifactured for NA62.

Conclusions

Quite independently from the final choice for the PP-FPGA devices, the new FPGAs and memories are not pin-compatible with the original ones and, together with the other modifications listed above, will require a significant redesign of a good part of the PCB. We plan to have the new PCB design made at CERN, by the same team who did this for the original TELL1. A discussion of board production and costs is outside the scope of this document.

Apart from the hardware upgrades discussed in this note, a significant amount of work will be required in terms of FPGA firmware. While some low-level parts of the firmware developed by LHCb might be re-used, a large fraction of it will have to be re-written (and simulated) within NA62 because of the different features required by the experiment: besides the need to handle

NA62-specific daughter cards (e.g. the TDC mezzanine), one can quote as an example the lack of working LHCb firmware for handling the external buffer memories. It should be pointed out that, even in case the TEL62 would be used with LHCb mezzanines, some work would be required to port the firmware to the new family of FPGAs. Experience was gained with the development of custom NA62 firmware for the original TELL1, used in beam tests in the past two years. Similar considerations apply to the control software running on the CCPC: using only low-level libraries developed by LHCb for hardware interface, the entire structure of the user-level code was rewritten within NA62, and a versatile scripting-capable command-line interface was developed.

References

[1] G. Haefeli *et al.* - TELL1 Specification for a common read out board for LHCb – LHCb note LHCb 2003-007, October 2003.