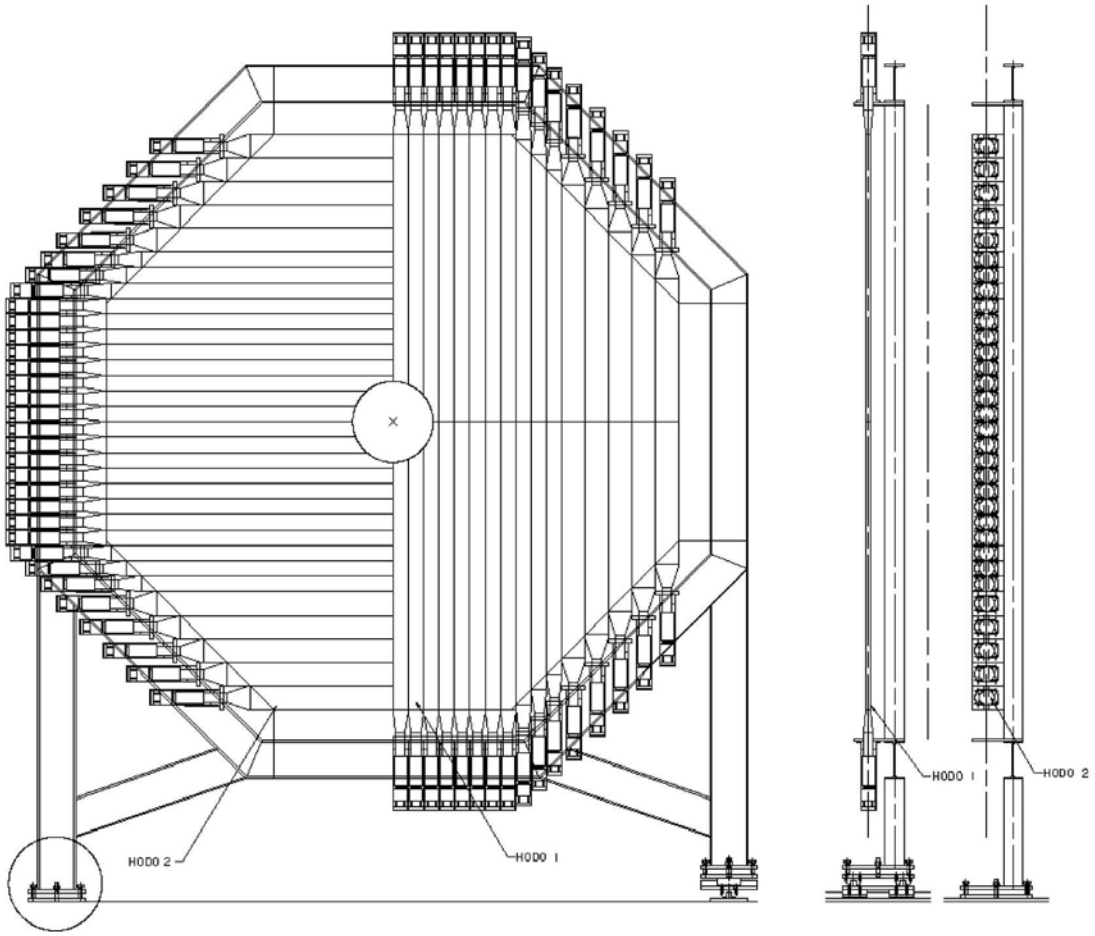

Figure 1 Schematic view of the CHOD detector

1.1 The CHOD

The existing NA48 charged hodoscope is a system of scintillation counters with high granularity and excellent time resolution (200ps) (1). It will be re-used to detect possible photo-nuclear reaction in the RICH mirror plane and to back-up the RICH in the L0 trigger for charged tracks.

The detector consists of 128 detection channels which are arranged in two planes of 64 horizontal and vertical scintillators. Each plane is divided in four quadrants with 16 counters (see Figure 1), so that the acceptance in the X-Y plane covers a radius of 121 cm. The scintillator dimensions are summarized in Table 1.

The counters are made with BC408 plastic scintillators which have fast light output and good attenuation properties. The scintillation light from each counter is collected via a short fishtail, (made of Plexiglas) light guide, followed by a Photonis XP2262B photomultiplier. Table 1

Table 1 CHOD Scintillator Dimensions

Lengths:	Between 121 and 60 cm
Width:	6 cm
Thickness:	2 cm

The RICH mirror system amounts to about 20% of radiation length and photons from π^0 decays can convert or, even more critical, undergo photonuclear interactions producing low energy hadrons. The Liquid Krypton Calorimeter (LKR) -as subsequent photon detector- has to veto these photons with an inefficiency that is better than 10^{-5}. MC simulations show that photons - which experience photo-nuclear reactions in the RICH - can weaken the photon-veto function of the LKR. In order to re-establish the veto sensitivity to the required level a detector for low momentum charged track after the RICH is needed. This function can be fulfilled by the CHOD.

Another motivation for keeping the present CHOD detector is its timing capabilities, which can be useful in complementing the RICH detector in the L0 trigger selecting charged tracks. The time resolution of an individual plane remains, however, limited by the size and the age of the counters to a level between 3 and 5 ns. This resolution can be improved (drastically) if the two planes are used simultaneously to correct the timing with respect to the crossing point of the track.

The frontend and readout electronics of the CHOD detector have to be entirely re-done in order to cope with the particle flux rate in the CHOD, which is estimated to be around 11 MHz. At this stage several options are under and the choice will depend on the facilities needed for the trigger.

Bibliography

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NA62 Acronyms and Abbreviations

ADC	Analog to Digital Converter
AM	Absorber Module
APD	Avalanche PhotoDiode
ASIC	Application Specifc Integrated Circuit
BCRST	Bunch Counter ReSeT
BEATCH	Progran to provide coordinates of all beam elements as input for alignment
BEND	BENDing magnet or dipole
BIF	Barrier Improvement Factor
CALB	Sub-detector data format for calibration
CCPC	Credit-Card PC: commercial processor on TELL1/TEL62 boards
CEDAR	Cerenkov Differential counter with Achromatic Ring Focus: differential Cerenkov detector developed at CERN
CHANTI	Charged ANTI
CHOD	Charged HODoscope
CKM	Cabibbo–Kobayashi–Maskawa matrix
CM	Circulation Module
COLL	COLLimator
COND	Condition data of the detector (extracted from DCS)
CONF	configurations of the run, including active detectors, trigger configurations, beam conditions, etc.
COST	calibration parameters computed by calibration tasks running on (partially or fully) reconstructed data.
COTS	Commercial-Of-The-Shelf
CPD	Calorimeter Pipeline Digitizer module
CREAM	Calorimeter Readout Module
CTL	Chamber Trigger Logic for straws L0 trigger system
DAQ	Data Acquisition System
DCS	Detector Control System
DDR2	Double Data Rate SDRAM (memory chips)
DIM	Distributed Information Management system
DLL	Delay Locked Loop
DLS	Data Logging System
DM	Distribution Module
DPRAM	Dual Ported RAM
DRAM	Dynamic RAM
EB	Event-Building
ECN3	Experimental Cavern housing the NA62 experiment
ECRST	Event Counter ReSeT
EDX	Energy-Dispersive X-ray spectroscopy
EE	End of Ejection
EOB	End Of Burst
EOC	End Of Column option for GTK chip architecture

EoC	End-of-Column part in the P-TDC chip architecture of the GTK
EOF	End Of Frame
FADC	Flash Analog to Digital Converter
FE	Front-End
FEE	Front-End Electronics
FEM	Finite Element Model
FIFO	First In First Out buffer
FISC	Filament Scanner, a beam profile detector inside the beam vacuum system
FNAL-NICADD	Fermi Nat Lab - Photo injector Lab (18Mev electron linac)
FPGA	Field Programmable Gate Array
FR	Fast Reconstruction
GbE	Gigabit Ethernet
GIM	Glashow–Iliopoulos–Maiani mechanism which suppresses flavour-changing neutral currents)
GOL	Gigabit Optical Link transmitter
GPN	General Purpose Network
GPU	Graphic Processing Unit
GTK	GigaTracker
HALO	A beam simulation program to calculate muon HALO rates
HPTDC	High Performance Time to Digital Converter
HV	High Voltage
IRC	Intermediate Ring Calorimeter
JTAG	Joint Test Action Group protocol
L0	Level 0 Trigger
L0TP	Level 0 Trigger Processor
L1	Level 1 trigger
L1TP	Level 1 Trigger Processor
L2	Level 2 trigger
LAV	Large Angle Veto
LED	Light-Emitting Diode
LG	Lead Glass
LGTS	Lead Glass Test Station
LKr	Liquid Kripton calorimeter
LTU	Local Trigger Unit
LV	Low-Voltage
LVDS	Low-Voltage Differential Signalling
MBPL-TP	Dipole Bending Magnet with Tapered Pole
MEPs	Multi-Event Packets
MIP	Minimum ionising particle
MNP33	NA62 Experimental Magnet
MUV	Muon Veto System
NAHIF	North Area High Intensity Facility
NIM	Nuclear Instrumentation Module
NINO	Fast front-end preamplifier-discriminator chip developed by ALICE
NNLO	Next-to-next -to-leading order
PCB	Printed Circuit Board

PDE	Photon Detection Eff.
Pe	Photo-electron
PECL	Positive Emitter-Coupled Logic
PEI	PolyEtherImide
PET	PolyEthylene Terephthalate
PMT or PM	Photomultiplier Tube
POPOP	1,4-bis(5-phenyloxazol-2-yl) benzene organic scintillator
PP-FPGA	Pre-Processing FPGA in the TELL1/TEL62 boards
PPO	2,5-Diphenyloxazole organic scintillator
PTP	Para-TerPhenyl
PVSS	Object-oriented process visualization and control system by ETM (a commercial SCADA system)
QCD	Quanten Chromodynamik
QDR-II	Quad Data Rate II memory
QPLL	Quartz-crystal based Phase-Lock Loop
QUAD	QUADrupole
RECO	Data format for fully reconstructed events
RICH	Ring Imaging Cherenkov
SAC	Small Angle Calorimeter
SAV	Small Angle Veto
SDRAM	Synchronous Dynamic Random Access Memory
SEM	Scanning Electron Microscope
SiPM	Silicon PhotoMultiplier
SOB	Start of Burst
SL-FPGA	Sync-Link FPGA in the TELL1/TEL62 boards
SLM	Smart Link Modules
SM	Standard Model of particle physics
SPI	Serial Port Interface
SPR	Single Photoelectron Response
SRAM	Static Random Access Memory
SRB	Straw Readout Board
TCC8	Target Chamber Cavern upstream of ECN3
TDAQ	Trigger and Data Acquisition system
TDC	Time to Digital Converter
TDCB	Time to Digital Converter Board
TDCC-FPGA	TDC Controller FPGA in the TDC boards
TEL62	Trigger and Data Acquisition board developed for NA62, based on TELL1 design
TELL1	Trigger ELectronics for L1 trigger: readout board developed by LHCb
THIN	Data format for summary data from fully reconstructed events
TRIM	Steering Magnets for the Beam
TTC	Timing, Trigger and Control
TTCex	TTC encoder VME board developed by CERN
TTCrq	TTC receiver mezzanine card developed by CERN
TTCrx	TTC receiver ASIC developed by CERN
TURTLE	Trace Unlimited Rays Through Lumped Elements, a beam tracking and simulation program

VME	Electronic bus and rack standard
VTL	View Trigger Logic for straws L0 trigger system
WE	Warning of Ejection
WLS	Wave-Length Shifting
WWE	Warning of Warning of Ejection